Study of Program Defects of 22nm Nano Imprint Template with an Advanced e-beam Inspection System

Takaaki Hiraka[1)], Jun Mizuochi[1)], Yuko Nakanishi[1)], Satoshi Yusa[1)], Shiho Sasaki[1)], Masaaki Kurihara[1)], Nobuhito Toyama[2)], Yasutaka Morikawa[3)], Hiroshi Mohri[3)], Naoya Hayashi[1)], Hong Xiao[4)], Chiyan Kuan[4)], Fei Wang[4)], Long (Eric) Ma[4)], Yan Zhao[4)], Jack Jau[4)]

1) Electronic Device Operations, Dai Nippon Printing Co., Ltd.
2-2-1, Fukuoka, Fujimino-shi, Saitama, 356-8507, Japan
2) Electronic Device Labs, DNP Corporation USA
3235 Kifer Road, Suite 100
Santa Clara, CA 95051
3) Electronic Device Lab, Electronic Device Operations, Dai Nippon Printing Co., Ltd.
2-2-1, Fukuoka, Fujimino-shi, Saitama, 356-8507, Japan
4) Hermes Microvision, Inc.
1762 Automation Parkway, San Jose, CA 95131

ABSTRACT

Nanoimprint lithography (NIL) is a candidate of alternative, low cost of ownership lithography solution for deep nano-meter device manufacturing[12]. For the NIL template pattern making, we have been developing the processes with 100keV SB EB writer and 50keV VSB EB writer to achieve the fine resolution of near 20nm[1-7]. However, inspection of nanoimprint template posed a big challenge to inspection system due to the small geometry, 1x comparing to 4x of Optical mask and EUV mask. Previous studies of nanoimprint template inspection were performed indirectly on a stamped wafer and/or on a round quartz wafer[13]. Electron beam inspection (EBI) systems have been widely used in semiconductor fabs in nanometer technology nodes. Most commonly EBI applications are electrical defects, or voltage contrast (VC) defects detection and monitoring[8-11].

In this study, we used a mask EBI system developed by Hermes Microvision, Inc. (HMI) to directly inspect a NIL template with line/space and hole patterns half pitched from 22nm to 90nm and with program defects sized from 4nm to 92nm. Capability of inspection with 10nm pixel size has been demonstrated and capability of capturing program defects sized 12nm and smaller has been shown. This study proved the feasibility of EBI as inspection solution of nanoimprint template for 22nmHP and beyond.

Key word: NIL, Template, Defect inspection, EBI

1. INTRODUCTION

NIL templates have 1X patterns and are required manufacturing process with higher resolution compared to that of the 4X photomasks. Table 1 shows the ITRS requirements on masks for NIL, EUV, and optical lithography. Although the patterns on the NIL templates will be made by the EB writing process as shown in Figure 1, which will also be used for advanced photomasks, the resolution should be finer and close to 20nm in year 2013. The minimum allowed defect size on the template is also be tough and is different from other masks, and many efforts should be paid.

For the NIL template pattern making, we have been evaluating two different processes, one with the 100keV SB EB writer, and the other with the 50keV VSB EB writers[1-7]. The 100keV SB writer has high resolution capability down to 15nm, as shown in Figure 2. But it has a fatally low throughput for full field writing. On the other hand, the 50keV

VSB writer is actually used in today's photomask manufacturing, and can write full field in a reasonable time. They are designed for 4X pattern, but with the continuous improvement of resist process for 1x template application, we can have the resolution close to 20nm, as shown in Figure 3.

Figure 4 shows the CD uniformity results in the active area (30x26mm) and the quartz depth uniformity results in the active area of NIL templates with 50keV VSB EB writer. The CD and quartz depth were measured at 32nm patterns. The CD uniformity result was 1.2nm in 3σ which met the ITRS requirement of 3.1nm, and the quartz depth uniformity was 0.8nm in 3 σ and also met the ITRS requirement of 2.1nm.

Figure 5 shows the image placement accuracy results in the active area. The image placement accuracy (3σ) results were X: 2.9nm, Y: 4.2nm, and X: 6.0nm, Y: 6.0nm with 50keV VSB EB writer and 100keV SB EB writer, respectively. These values did not meet the ITRS requirement of 3.7nm. We believe the image placement accuracy result with 50keV VSB EB writer show a sufficient value for the time being, and will be improved along with the coming technology nodes 4X photomask manufacturing.

Defect control is the most challenging issue for NIL template based on the specification requirement of ITRS roadmap. To get the finer resolution, E-Beam inspection (EBI) tool is the candidate to capture the defect on the pattern. There are several EBI tools for wafer on which the pattern were printed[14]. Because of quartz substrate, NIL template may have the charging issue with EBI. We have been evaluating EBI tool especially designed for mask inspection from HMI for direct template defect inspection.

2. EXPERIMENTAL

Table 2 shows the experimental tools and material. We used the "JBX9300" (JEOL) as the 100keV SB EB writer. As the 50keV VSB EB writers, machines used in current 4X photomask manufacturing were used. A positive tone non-CAR (non-chemically amplified resist) was used as the resist material. For measurement tools, we used "LWM9000" (Vistec) CD-SEM, "LMS IPRO" (Vistec) image placement measurement tool, "Dimension X3D" (Veeco) AFM. Imprint performance test was done by an "Imprio250" (Molecular Imprints Inc) tool.

Mask EBI system, eXplore™ 5200 of Hermes Microvision Inc., was used as template defect inspection tool. This system has 10nm minimum pixel size, leap and scan mode for high resolution, and continuous scan mode for higher throughput. We used leap and scan mode with 10nm pixel size for this study.

Defect sizes were calculated of root square of measured defect area from CD-SEM figures.

3. RESULTS AND DISCUSSION

3-1. Programmed defect template for evaluation

Figure 6 shows the design and layout of programmed defect template. Figure 7 shows the results of programmed defect and natural process defect on 22nmHP line and space pattern on the template. We had large number of process defects on 22nmHP line and space pattern because of process limitation on smallest patterns. We are considering that whether or both of a new resist system and a new writing strategy might be necessary for further improvement. We used relatively larger patterns, 26nmHP and 28nmHP, for defect inspection tool evaluation this time.

3-2. Defect inspection results on line and space patterns

Figure 8 show the inspection results on 26nm 1:1 line and space. Excessive defects of 16nm designed size were all captured, which were measured about 30nm actual defect size (Defect sizes were calculated of root square of measured defect area from CD-SEM figures). Missing defects of 12nm designed size, which were measured about 20nm actual defect size and CD defect of 8nm designed size were also captured. Because of poor linearity between designed defect size and actual defect size, we could not confirm the inspection capability below 20nm. Because of dense pattern, it seems difficult to get the linearity of defect size on the pattern edge.

Figure 9 show the results on 26nm 1:3 line and space. One of the excessive defects on the pattern edge, which was measured about 15nm actual defect size, was captured. Missing defects of about 30nm actual defect size were also

captured. However, we could not confirm the inspection capability below 20nm even those semi-dense patterns. On the other hand, CD defect of 4nm designed size was captured.

Figure 10 show the results on 28nm 1:1 line and space. Those results are as same as 26nm patterns.

Figure 11 show the results on 28nm 1:3 line and space. Those results are also as same as 26nm patterns.

We need further improvement of the template process to get the linearity on actual defect sizes, and inspection condition optimization to confirm the inspection capability below 20nm in future.

3-3. Defect inspection results on hole array patterns

Figure 12 shows the results on 26nm 1:1 hole array. Most of 16nm designed defects were captured, but as you can see in those "captured" and "missed" features, it seems difficult to define the actual defect size. Most of defects were connected to be a large hole or nothing there.

Figure 13 shows the results on 26nm 1:3 hole array. Most of 12nm designed defects were captured, but definition of actual defect sizes remained the issue as same as previous result.

3-4. Captured defect summary

Table 3 shows the summary of captured defect size on various designed line and space patterns. Again, we found the possibility of inspection sensitivity of around 20nm, but need further investigation with improvement on template process.

We will continue to evaluate the EB inspection system for NIL templates and will report on our next paper.

4. SUMMARY

We have been developing NIL templates using and modifying current photomask manufacturing technology. Line and space test pattern down to 15nmHP was resolved with a 100keV spot beam EB writer, and with a 50keV variable shaped beam EB writer, we could resolve line and space pattern down to 22nmHP. With 50keV EB writer process, CD uniformity, quartz depth uniformity, and image placement are satisfied or closed for ITRS requirements at 2013, 32nmHP.

We have preliminarily evaluated template defect inspection capability with an EB inspection method using a programmed defect template. With an HMI EB inspection system we have seen promising results. But we still have some gap between the requirement and current capability. We are planning to do further study in future with optimized template processes for improved programmed defect template, and also fine tuned inspection conditions on EB inspection tool to fill the gap.

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REFFERENCE

[1]. S. Yusa, T. Hiraka, A. Kobiki, S. Sasaki, K. Itoh, N. Toyama, H. Mohri, N. Hayashi, "Progress of NIL template making", Proceeding of SPIE, Vol. 6607, p. 66073H ,2007.

[2]. T. Hiraka, S. Yusa, A. Fujii, S. Sasaki, K. Itoh, N. Toyama, M. Kurihara, H. Mohri, N. Hayashi, "UV-NIL template for the 22nm node and beyond", Proceeding of SPIE, Vol.6730, p.67305P (2007).

[3]. S. Yusa, T. Hiraka, J. Mizuochi, A. Fujii, Y. Sakai, K. Kuriyama, M. Sakaki, S. Sasaki, Y. Morikawa, H. Mohri, N.

Hayashi, “Progress of NIL template making”, Proceeding of EMLC2008, p.23-34 (2008).
[4]. A. Fujii, Y. Sakai, J. Mizuochi, T. Hiraka, S. Yusa, K. Kuriyama, M. Sakaki, T. Sutou, S. Sasaki, Y. Morikawa, H. Mohri, N. Hayashi, “UV NIL mask making and imprint evaluation” , Proceeding of SPIE, Vol.7028, p.70281W (2008).
[5]. S. Sasaki, T. Hiraka, J. Mizuochi, A. Fujii, Y. Sakai, T. Sutou, S. Yusa, K. Kuriyama, M. Sakaki, Y. Morikawa, H. Mohri, and N. Hayashi, “UV NIL template making and imprint evaluation”, Proceeding of SPIE, Vol.7122, p. 71223P-1 (2008).
[6]. S. Sasaki, T. Hiraka, J. Mizuochi, Y. Sakai, S. Yusa, Y. Morikawa, H. Mohri, and N. Hayashi, “UV NIL template making and imprint evaluation”, EMLC 2009 (2009).
[7]. T. Hiraka, J. Mizuochi, Y. Nakanishi, S. Yusa, S. Sasaki, Y. Morikawa, H. Mohri, and N. Hayashi, “Progress of UV-NIL template making”, PMJ2009, SPIE Vol.7379, 73792S-1 (2009).
[8] Jean-Luc Baltzinger, Stephanie DesmerciBres, SBbastien Lasserre, Patrick Champonnois, Michele Mercier, “E-beam inspection of dislocations: product monitoring and process change validation” Proc. of IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 361 (2004).
[9] Kirin Wang, Hermes Liu, J. H. Yeh, Mingsheng Tsai, Wei-Yih Wu, Hong-Chi Wu, Hong Xiao and Jack Jau, “Post-WCMP Leakage Detection and Monitoring on 65-nm Devices Using an Advanced e-beam Inspection System”, Proc. of IEEE International Symposium of Semiconductor Manufacturing, pp. 472 (2005).
[10] Shuen-chen Lei, Hermes Liu, Mingsheng Tsai, Hung-Chi Wu, Hong Xiao and Jack Jau, “Contact leakage and open monitoring with an advanced e-beam inspection system”, Proc. of SPIE, Vol. 6518, pp. 65184I (2007).
[11] Li-Lung Lai, Keren Xu, Daniel Deng, Jay Ning, Hong Xiao, Yan Zhao, Eric Ma, and Jack Jau, “Mechanism and Application of Negative Charging Mode of Electron Beam Inspection for PMOS Leakage Detection”, Proc. of IEEE International Interconnect Technology Conf., pp. 111 (2007).
[12] http://public.itrs.net/
[13] L. Jeff Myron, Ecron Thompson, Ian McMackin, Douglas J. Resnick, Tadashi Kitamura, Toshiaki Hasebe, Shinichi Nakazawa, Toshifumi Tokumoto, Eric Ainley, Kevin Nordquist, William J. Dauksher, “Defect Inspection for Imprint Lithography Using a Die to Database Electron Beam Verification System”, Proc. of SPIE Vol. 6151, 61510M (2006)
[14] Kosta Selinidis, Ecron Thompson, S. V. Sreenivasan, Douglas J. Resnick, Marcus Pritschow, Joerg Butschke, Mathias Irmscher, Holger Sailer, Harald Dobberstein, “Inspection and Repair of Imprint Masks at 32nm and Below”, PMJ2009, SPIE Vol.7379, 73790N-1(2009)

Table. 1 The requirements on masks from ITRS2008

Year of Production	**2013**		
DRAM 1/2pitch	32		
Flash 1/2pitch	25		
MPU Gate in resist	25		
DRAM/FRASH CD control (3σ)	3.3		
Gate CD control (3σ)	1.9		
Overlay (3σ)	6.4		
MASK (template) requirement	**NIL**	EUVL	Optical
Magnification	1	4	4
MASK nominal image size	25	100	70
Image placement (nm, multipoint)	3.7	3.8	3.8
CDU Isolated lines (MPU gates)	1.8	2.8	1.4
CDU Dense line DRAM/FRASH(half pitch)	3.1	4.6	2.4
CDU Contact/vias	3.5	3.5	1.3
Etch depth uniformity	2.1-3.2		
Trench width roughness (3σ)	2.2		
Defect size impacting CD x,y	2.5	25	25
Defect size impacting CD z	5.1		

Figure. 1 UV-NIL template process flow

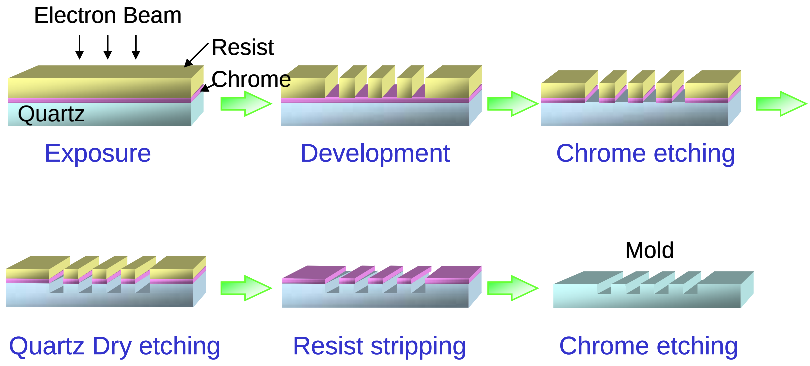


Figure. 2 Resolution of resist images with 100KeV EB Writer

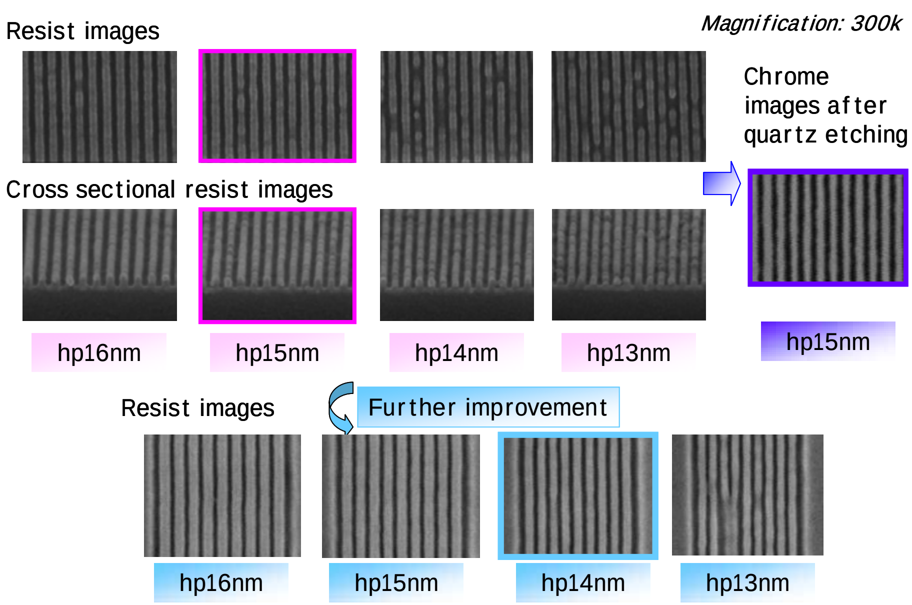


Figure. 3 Resolution of etched quartz images with 50KeV EB Writer

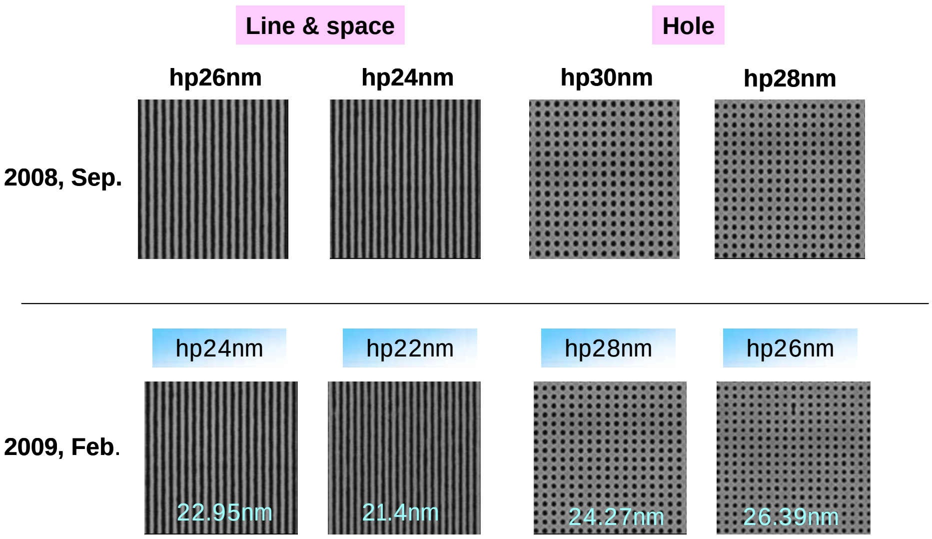


Table. 2 Tools and material

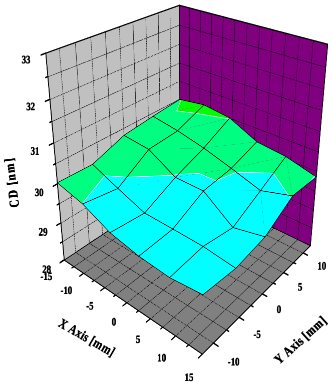
EB writing tool	100keV Spot Beam writer : JBX9300 50keV Variable Shaped Beam (VSB) writer : photomask production tool
Resist material	Non-CAR (positive-tone)
Measurement tools	CD-SEM (LWM9000) Image placement (LMS IPRO) AFM (Dimension X3D)
EB inspection tool	eXplore 5200 (Hermes Microvision Inc.)

Figure. 4 CD uniformity and quartz depth uniformity

Area : 30 x 24mm (6 x 5 measurement array)

CD uniformity

HP32nm dense lines

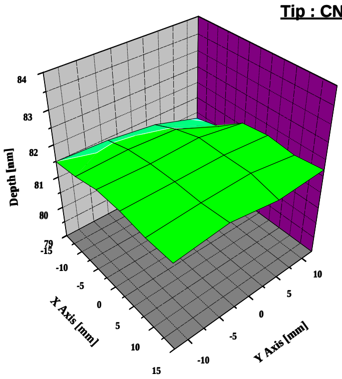


Average : 29.9nm
Range : 1.3nm
3σ : 1.2nm

Quartz depth uniformity

32nm iso space

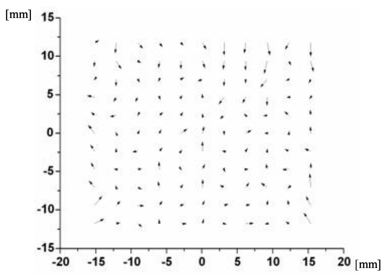
Tip : CNT probe



Average : 81.6nm
Range : 1.2nm
3σ : 0.8nm

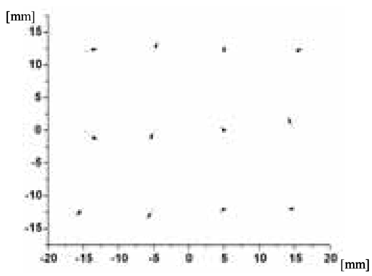
Figure. 5 Image Placement Accuracy results

50keV VSB
Area 30 x 26 mm (11 x 11 arrays)



	X	Y
3σ	2.9	4.2
Min	-2.0	-3.0
Max	2.0	4.0

100keV SB
Area 28 x 24 mm (5 x 3 arrays)



	X	Y
3σ	6.0	6.0
Min	-2.0	-3.0
Max	4.0	4.0

Figure. 6 Design and layout of programmed defect template

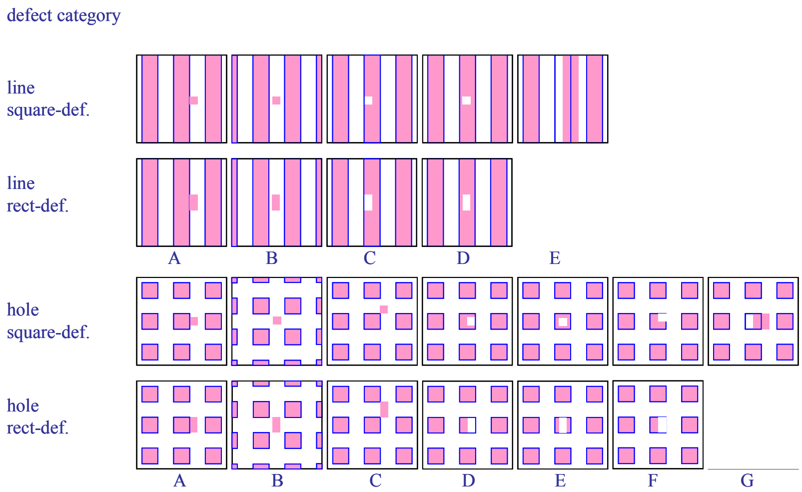


Figure. 7 Programmed defect and process defects on 22nmHP

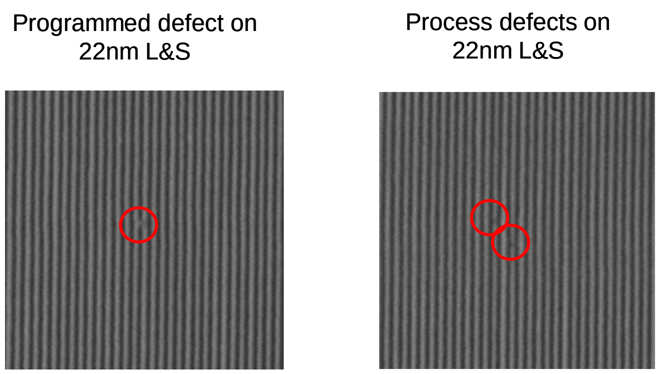


Figure. 8 Inspection results on 26nmHP, 1:1 Lines and Spaces

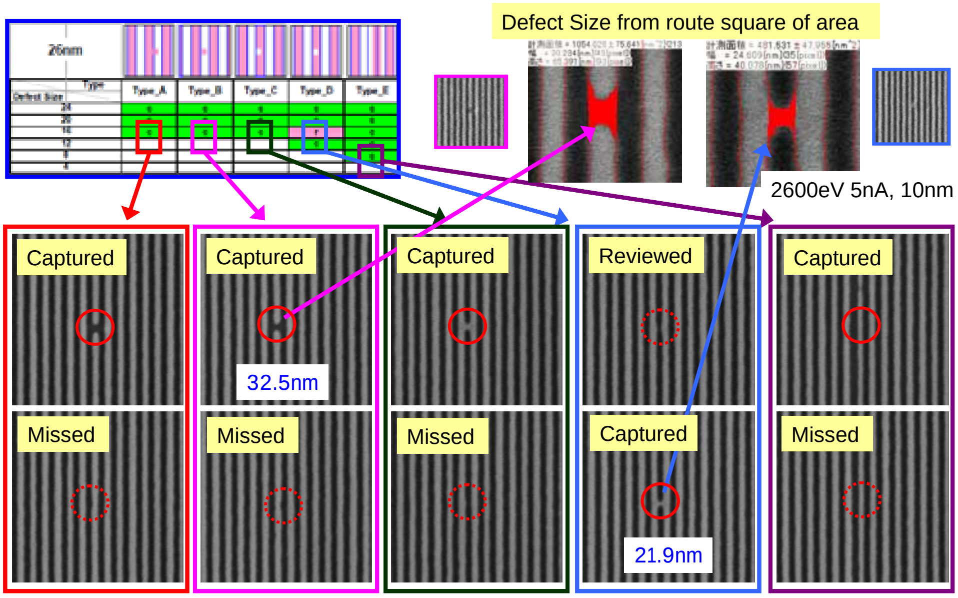


Figure. 9 Inspection results on 26nmHP, 1:3 Lines and Spaces

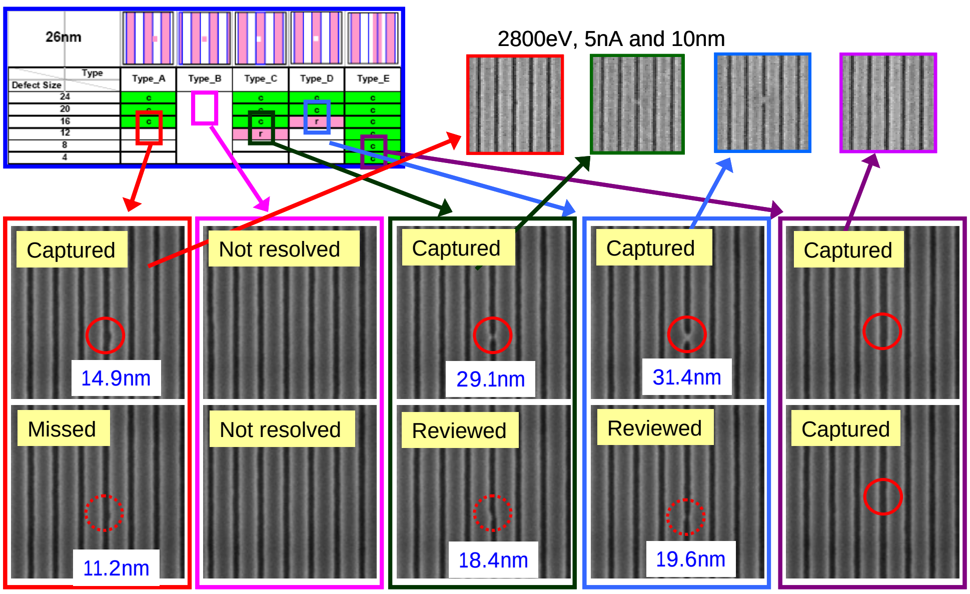


Figure. 10 Inspection results on 28nmHP, 1:1 Lines and Spaces

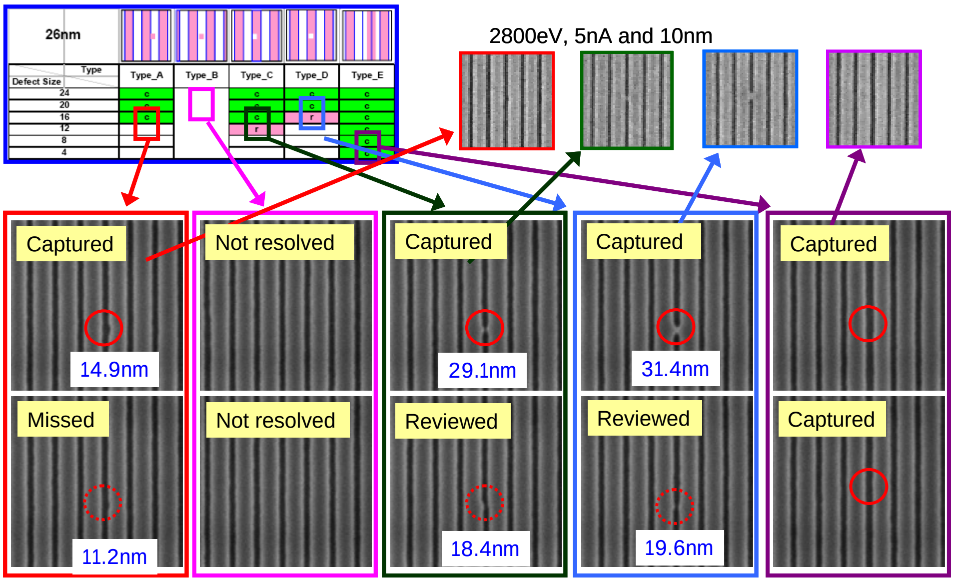


Figure. 11 Inspection results on 28nmHP, 1:3 Lines and Spaces

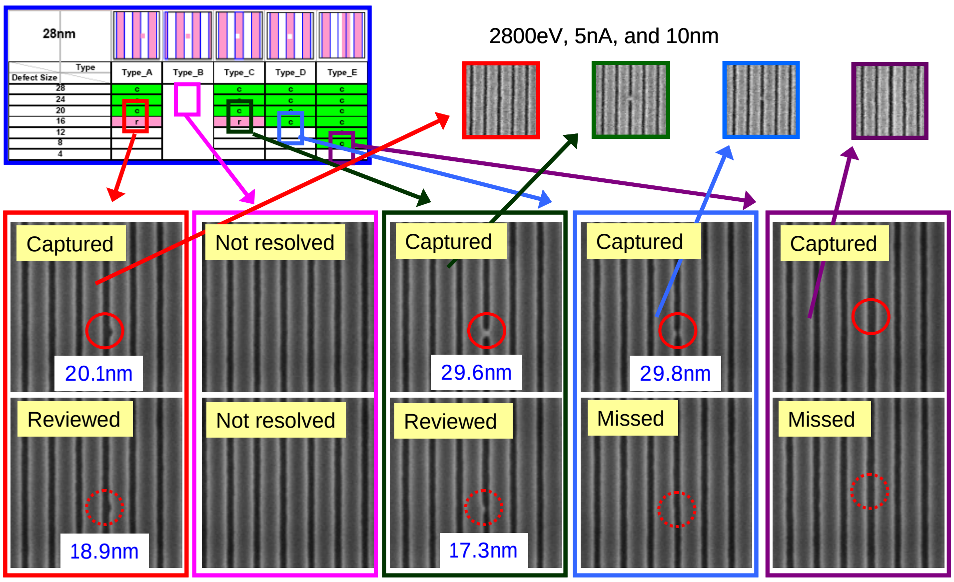


Figure. 12 Inspection results on 26nmHP, 1:1 Hole array

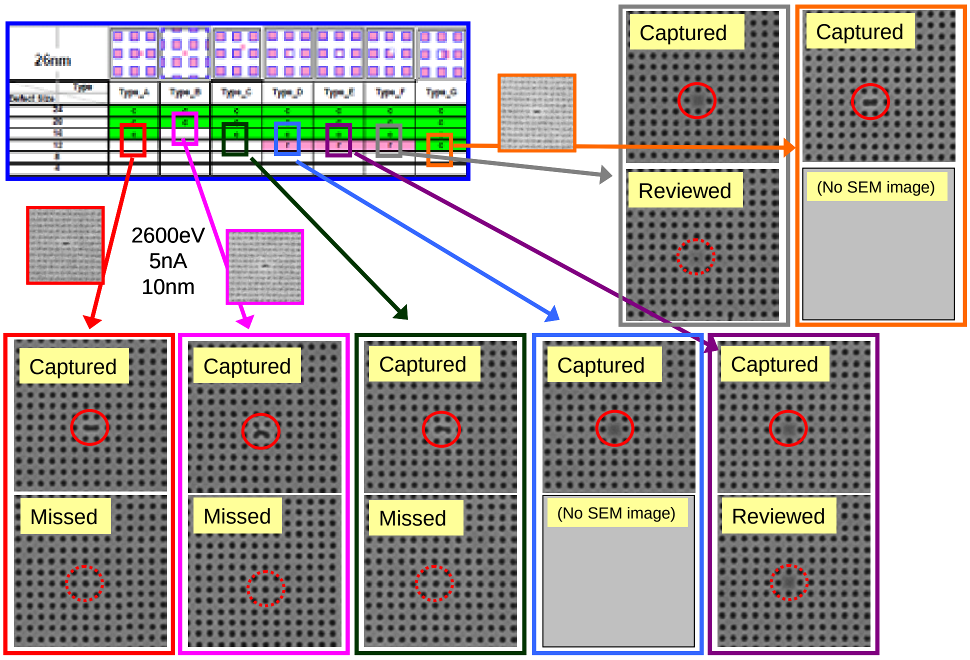


Figure. 13 Inspection results on 28nmHP, 1:3 Hole array

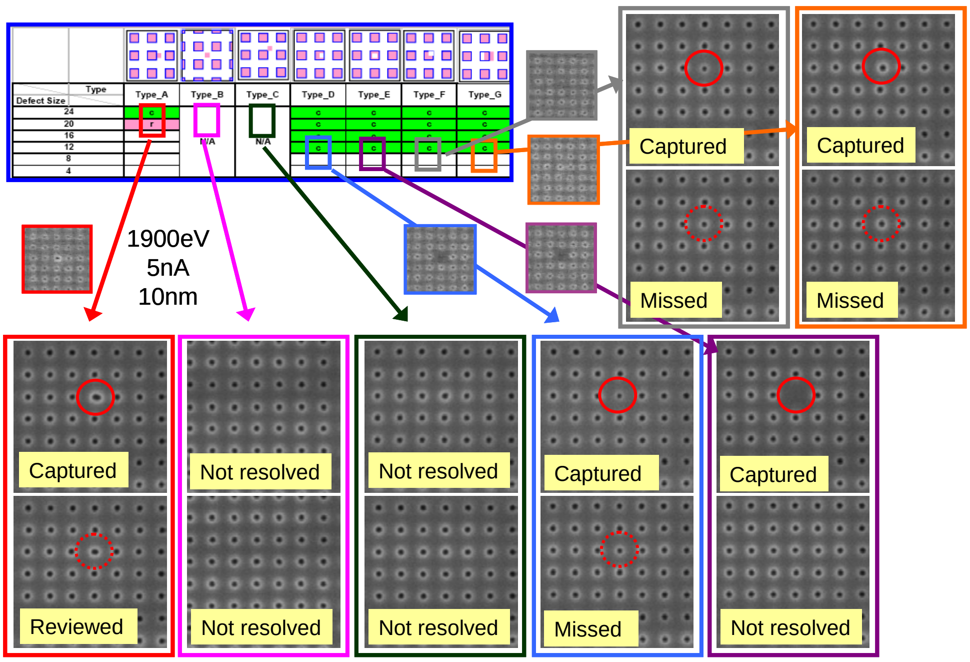


Table. 3 Summary of captured defect sizes

	Dense 1:1		Semi-dense 1:3	
	Clear	Opaque	Clear	Opaque
26nm L&S	33	22	15	30
28nm L&S	22	30	20	30

(nm)