Study of Devices Leakage of 45nm node with Different SRAM Layouts Using an Advanced e-beam Inspection Systems

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Abstract – In this study, a nickel silicide (NiSi) wafer and a WCMP wafer were used. We captured bright voltage contract (BVC) defects at N+/P-well on NiSi wafer, we also captured N+/P-well leak/short defects on WCMP wafer as BVC defects in positive mode inspection and dark voltage contrast (DVC) defects in Negative Mode™ inspection. N+/P-well leakage signatures of the two inspection modes of WCMP strongly correlate with each other, which indicate they are the same defects. N+/P-well leakage signature on WCMP wafer also correlate with that on NiSi wafer. With negative mode inspection, we captured P+/N-well leakage on WCMP wafer at two different static random access memory (SRAM) arrays (SRAM1 and SRAM3) as DVC defects. The P+/N-well leakage signature is very different from N+/P-well leakage signature in SRAM3. P+/N-well leakage signature of SRAM1 is also very different from that of SRAM3. This study confirmed our prediction that different SRAM layout will cause different P+/N-well leakage, especially in the case of over etching of share contact hole.

Introduction

Electron beam (e-beam) defect inspection becomes more and more important when integrated circuit (IC) manufacturing entering nanometer technology node. [1], [2] Nickel silicide (NiSi) became widely adapted in logic IC devices from 65nm technology node, NiSi-induced device leakage becomes more challenge when device dimension shrinks. [3] e-beam inspection (EBI) is widely used after contact tungsten chemical mechanical polishing (WCMP) to capture and monitor leakage caused by NiSi encroachment and NiSi piping. [2] As device dimension shrinking, there is a strong demand from IC manufacturers to capture this defect as early as possible, preferably right after NiSi formation. We studied n-type metal oxide semiconductor field effect transistor (nMOSFET or NMOS) leakage inspection on NiSi layer and compared the results with NMOS leakage EBI on WCMP layer.

Start from 65 nm technology node, we observed several different leakage mechanisms of P+/N-well of p-channel metal-oxide-semiconductor field effect transistor (pMOSFET or PMOS), such as W spiking caused by over etch [4] and NiSi spiking likely caused by photo-electro-chemistry. [5] For advanced static random access memory (SRAM), over etch induced PMOS leakage is related to its layout. Figure 1a illustrates a layout of SRAM that has high risk of PMOS leakage caused by over etching induced W spiking, because the share contact touched the STI oxide. Figure 1b illustrates the SRAM array that has less such risk. Gate to active area (AA)

overlay shift could also make exposure of STI oxide to contact etch and increase risk of W spiking. To avoid W spiking caused by excessive oxide loss, selectivity of oxide to silicon in over etch step of the contact etching needs to be adjusted to ~1. However, it can also cause PMOS leakage when contact hole etch through the P-type source/drain junction. In this work, we studied PMOS leakage using Negative Mode^{TM} EBI on a 45nm WCMP wafer.

Experiment 1: PMOS Leakage

In this study, we used eScanLite® of Hermes Microvision, Inc. (HMI) to run Negative Mode^{TM} inspections of two SRAM arrays, SRAM1 and SRAM3 in a 45nm WCMP wafer. Figure 2 is the optical image of the two SRAM arrays. The EBI conditions are landing energy (LE) 3000eV, beam current 100nA, and pixel size 40nm. We have successfully captured P+/N-well leakage as dark voltage contrast (DVC) defects. The DVC defect map and total defect number of SRAM1 and SRAM3 are shown in Figure 3a and 3b, respectively. The defect maps show that SRAM1 P+/N-well leakage has a strong horseshoe style signature, while SRAM3 P+/N-well is pretty random with a little right side (notch down orientation) signature. The defect density of SRAM1 is much higher than that of SRAM3; the ratio of average defect density of SRAM1 to SRAM3 is about 360:1. Figure 4a, 4b and 4b are the review images of the P+/N-well DVC defects at SRAM1 site 1, SRAM1 site 2, and SRAM3, respectively. Both review images are taken with pixel size of 20nm. From Figure 4a and 4c we can see that both SRAM1 and SRAM3 have 11 and half pairs of pass gate plugs, indicates the device densities in x-direction are the same. However, SRAM1 has 10 rows pass gate plugs while SRAM3 has 12 and half rows, indicates that SRAM3 is denser in y-direction than SRAM1. This can help us to explain the image difference around the pass gates. Because the two rows of N+/P-well plugs are closer in SRAM3, the dark rings around NMOS plugs merges that causes the oxide becomes dark around the pass gate plugs between the two rows of N+/P-well contact plugs. For SRAM1, because the distance between the two rows of N+/P-well plugs is larger, and the dark rings of each row are separated, and oxide around the pass gate plugs is relatively bright.

We did the failure analysis (FA) on two sites of SRAM1 and one site of SRAM3. Tunneling electron microscope (TEM) images of defects in Site 1 of SRAM1, Site 2 of SRAM1, and SRAM3 are shown in Figure 5a, 5b, and 5c, respectively. From Figure 5a, we can see that at the Site 1, in the horseshoe of Figure 3a, the P+/N-well leakage is caused by over etching of the share contact, which shorts the P+ source/drain (S/D) junction and the N-well after W plug formation. Figure 5b shows the P+/N-well leakage is caused by NiSi piping underneath the spacer that shorts the (S/D) to the N-well. Figure 5c shows the TEM image of the P+/N-well DVC of SRAM3. We can see that the leakage is also caused by over etch of the share contact. Table 1 shows the energy dispersive X-ray (EDX) spectroscopy data collected from the defect site in Figure 5b, which confirmed the defect is NiSi piping.

In SRAM1 Negative Mode^{TM} inspection, we have also captured DVC on N+/P-well plugs, which indicate the short of N+ junction to the P-well and P-type substrate. The defect inspection patch image is shown in Figure 6a and defect number and map is shown in Figure 6b. Comparing Figure 3a with Figure 6b, we found that in

SRAM1, P+/N-well leakage (DVC) defect density is much higher than N+/P-well leakage, and their signatures are not the same, indicating different leakage mechanism. As we discussed, P+/N-well leakage in SRAM1 is mainly caused by over etching of the share contact hole along with some NiSi piping, while the N+/P-well leakage is mainly caused by NiSi encroachment and piping, which will be discussed in next section.

Experiment 2: NMOS Leakage

In this study, we used two wafers that process in the same 45nm process flow, one stopped at NiSi and another one stopped at WCMP. The purpose of the study is to capture NiSi diffusion induced N+/P-well leakage at the earliest spot: right after NiSi formation. We did positive mode inspection on SRAM3 of the NiSi wafer. We also did both positive mode inspection and Negative Mode^{TM} inspection on SRAM3 of the WCMP wafer. We successfully captured N+/P-well leakage in NiSi wafer as BVC defects. We also captured N+/P-well leakage in WCMP wafer, as BVC defects in positive mode inspection and as DVC defects in Negative Mode^{TM} inspection. The inspection patch images of NiSi BVC, WCMP positive mode BVC and WCMP Negative Mode^{TM} DVC are shown in Figure 7a, 7b, and 7c, respectively. Defect maps of NiSi BVC, WCMP positive mode BVC and WCMP Negative Mode^{TM} DVC are shown in Figure 8a, 8b, and 8c, respectively. All three defects maps have strong right side signature with notch down wafer orientation, indicate that their defect mechanisms are related. The X-axis of Figure 9 is number of BVC defects of positive mode EBI of each die in Figure 8b and Y-axis of Figure 9 is number of DVC defects in Negative Mode^{TM} EBI of each die in Figure 8c. We found that N+/P-well leak/short defects of positive mode BVC and Negative Mode^{TM} DVC are highly correlated with R^2=0.999, indicated that they are the same defects: N+ junction short to the ground, likely caused by NiSi piping or encroachment.

Review images of NiSi N+/P-well BVC defect is shown in Figure 10a. During inspection, because the pass gates were biased positively, the n-channel of the NMOS were turned on, therefore, one N+/P-well leakage could cause surface potential drop of whole row of N+ junction with the common P-well and caused BVC of the row in the inspection defect patch image, as shown in Figure 7a. During review, the current density increased significantly, and charges have trouble to leak to ground through a tandem of turned on n-channels. Therefore, only leaked N+ junction and few junctions right next to it show BVC, as shown in Figure 10a. Figure 10b is the positive mode review image of N+/P-well leak/short captured as BVC by positive mode WCMP EBI. Figure 10c is the Negative Mode^{TM} review image of the same defect which shows out as DVC.

It was the first time we captured N+/P-well DVC defects in WCMP Negative Mode^{TM} EBI. Because N+/P-well junction would turn on when surface charged negatively to ~ –0.7V, the W plugs contact N+/P-well in Negative Mode^{TM} EBI are normally surrounded by a dark ring and it is difficult to capture leakage defect, which theoretically could make the ring a little darker. When N+ junction shorts to the ground and plugs surface potential changes from around –0.7V to 0V, N+/P-well plugs will show as DVC defects in Negative Mode^{TM} EBI. Thus we can confidently predict the NMOS leakage defect shown in Figure 10b and 10c is N+ junction short to P-well and p-type substrate.

We performed N+/P-well defect FA on both NiSi BVC and WCMP positive mode BVC. Figure 11a is the TEM image of defect shown in Figure 10a. It clearly shows the NiSi encroachment underneath the spacer that causes the leakage. Figure 11b is the defect shown in Figure 10b, which shows the NiSi piping due to dislocation that caused N+ junction short to the P-well and p-type substrate. From upper lest corner of Figure 10b, we can also see NiSi encroachment underneath spacer, similar to the ones in Figure 11a. In Figure 10b, that plug shows a weak BVC while the plug with NiSi piping shows a strong BVC.

Conclusion

In this study, we have captured N+/P-well leakage defects on both NiSi wafer and WCMP wafer. We also captured P+/N-well leakage with Negative Mode^{TM} inspection of WCMP wafer. TEM images showed that N+/P-well leakage defects were caused by NiSi encroachment and dislocation induced NiSi piping. TEM images also showed that P+/N-well leakage defects were caused by both over etching of share contact holes and NiSi piping. Different SRAM layouts have different effects of share contact over etching, thus different P+/N-well leakage signature. In the same SRAM array, N+/P-well leakage signature can be quite different from P+/N-well leakage signature due to different leakage mechanisms. Therefore, to control and monitor device leakage defects, we strongly recommend running EBI at NiSi to capture N+/P-well leakage at the earliest step. We also strongly recommend performing Negative Mode^{TM} inspection at WCMP layer to capture and control P+/N-well leakage, as well as N+/P-well contact open and poly-to-contact short, along with positive mode inspection at the same layer that captures and monitors N+/P-well leakage, gate leakage and P+/N-well contact open.

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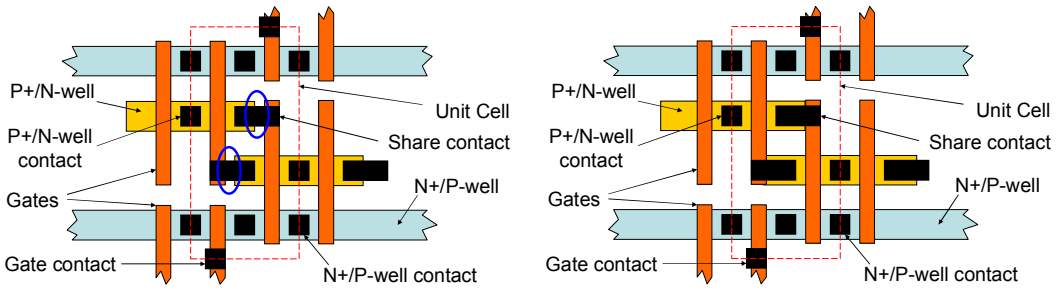
The samples were provided by one of leading IC manufacturers its in-house EBI systems had trouble to do negative mode inspection to capture PMOS leakage. Authors deeply appreciate its decision to allow us to publish the troubleshooting data and strictly follow its instruction not to disclose its identity.



(a) (b)

Figure 1. (a) Illustration of SRAM layout that has higher risk of overetch-induced PMOS leakage due to STI oxide exposed to the contact etch process. (b) Illustration of SRAM layout that has lower risk.

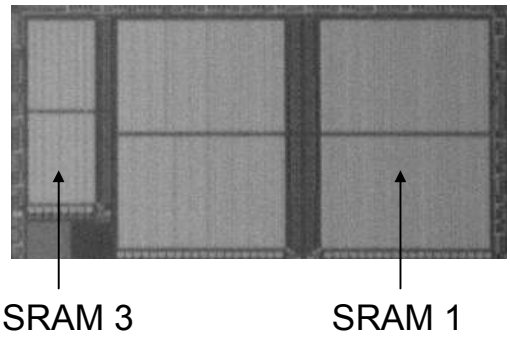
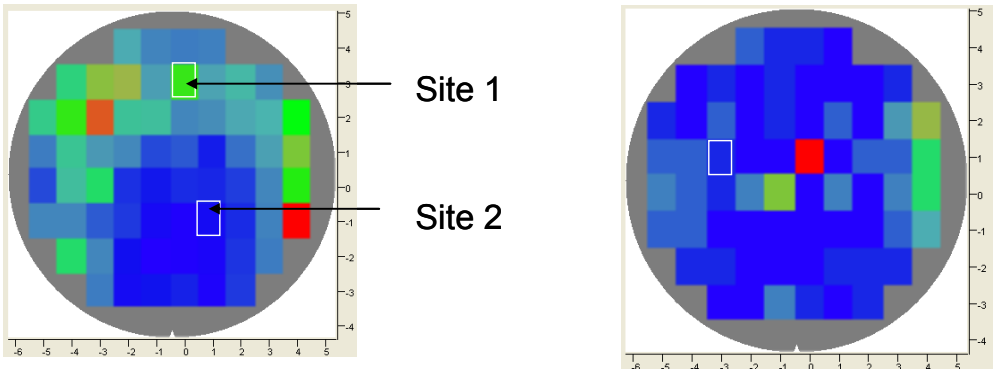


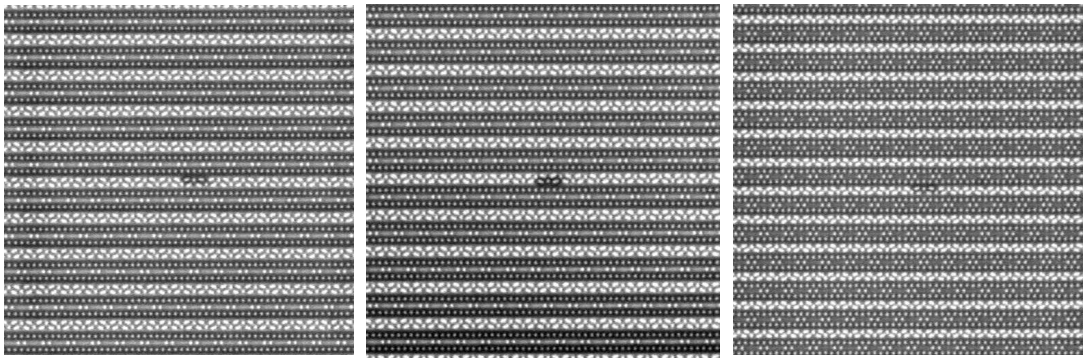
Figure 2. Optical image of SRAM 1 and SRAM 3.



52782 195

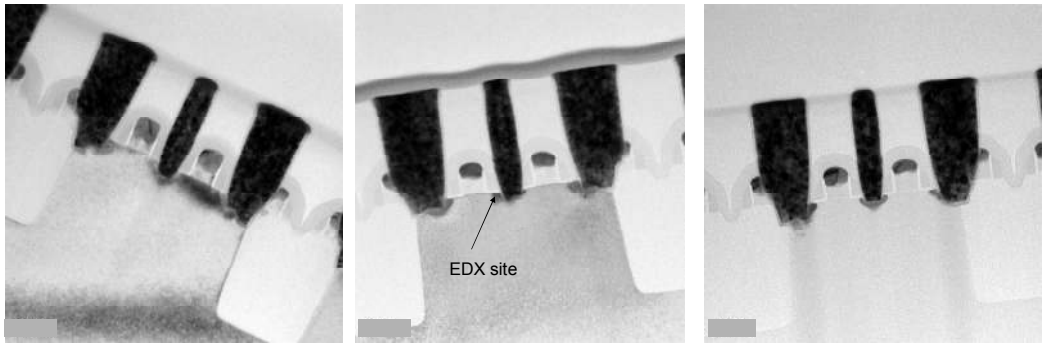
(a) (b)

Figure 3. P+/N-well leakage defect maps, FA sites, and total defect numbers of (a) SRAM1, (b) SRAM3. White dies with frame indicate the sites of FA.



(a) (b) (c)

Figure 4. Review images P+/N-well leakage defect. (a) SRAM1 site 1, (b) SRAM1 site 2, and (c) SRAM3.

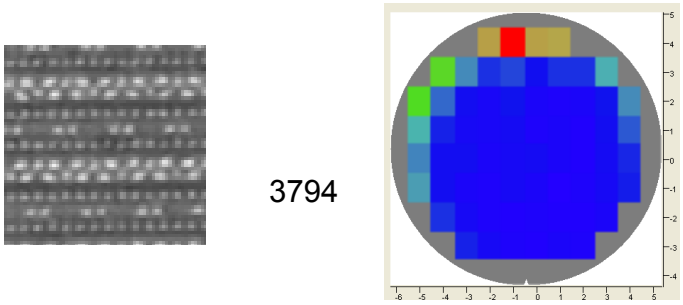


(a) (b) (c)

Figure 5. TEM images of P+/N-well leakage defects in (a) Site 1 of SRAM1, (b) Site 2 of SRAM1, and (c) SRAM3. Locations of these defects are shown in Figure 4a, 4b and 4c, respectively.

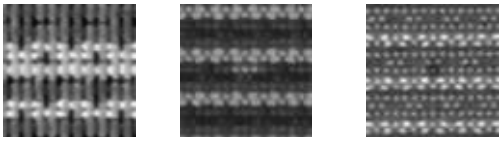
Element	Weight%	Atomic%
O K	9.89	17.83
Si K	70.81	72.69
Ni K	19.30	9.48
Totals	100.00	

Table 1. Defect EDX data at Site 2 of SRAM1.



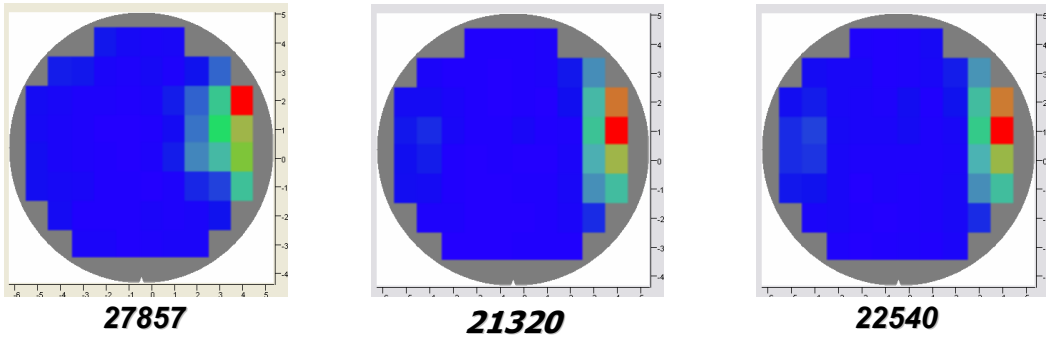
(a) (b)

Figure 6. Negative Mode™ EBI N+/P-well DVC defects in SRAM1. (a) defect patch image and (b) defect number and map.



(a) (b) (c)

Figure 7. Inspection patch images of N+/P-well leak/short defect in SRAM3. (a) NiSi EBI, (b) WCMP positive mode EBI, and (c) WCMP Negative Mode™ EBI.



(a) (b) (c)

Figure 8. SRAM 3 N+/P-well leak/short defect maps and numbers of (a) NiSi EBI, (b) WCMP positive mode EBI, and (c) WCMP Negative Mode™ EBI.

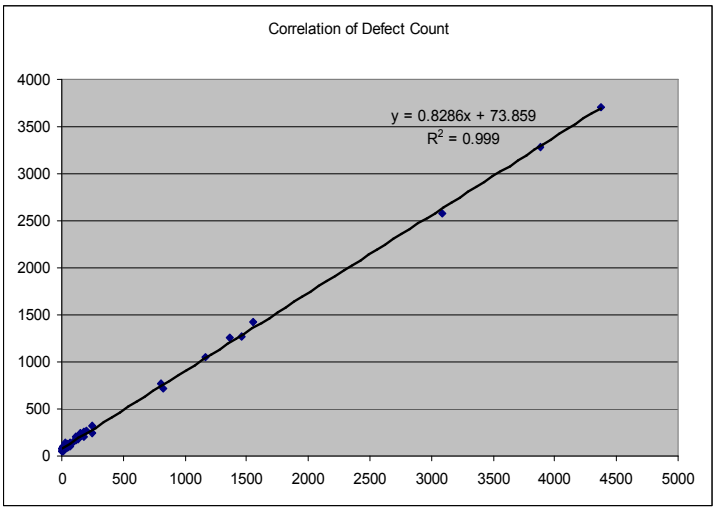
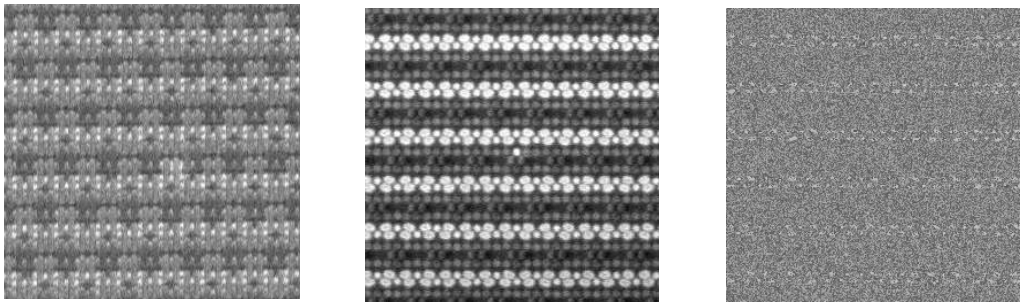
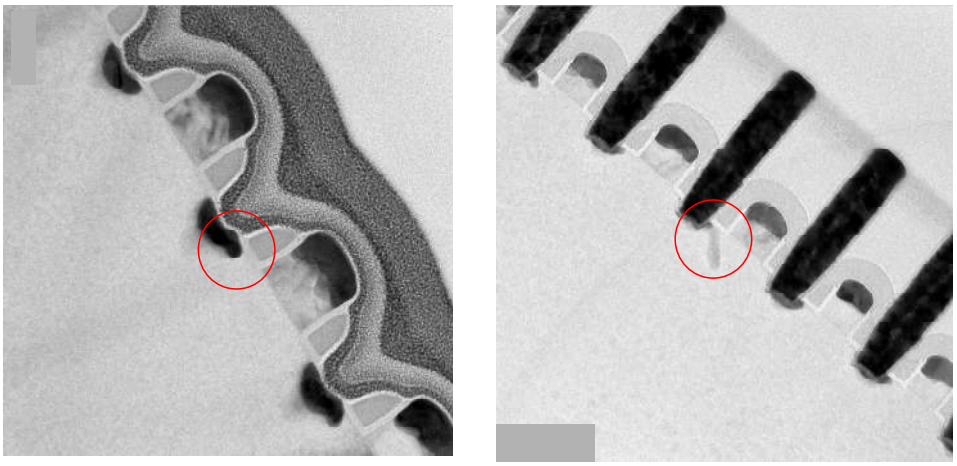


Figure 9. Correlation of N+/P-well leak/short defects per die.



(a) (b) (c)

Figure 10. Defect review images of SRAM3 N+/P-well leak/short. (a) NiSi BVC, (b) WCMP positive mode BVC, (c) Negative Mode™ DVC of the defect shown in (b).



(a) (b)

Figure 11. (a) TEM image of NiSi BVC defect shown in Figure 10a. (b) TEM image of WCMP positive mode BVC defect shown in Figure 10b.

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