Leakage Monitoring and Control with an Advanced e-Beam Inspection System

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Abstract – Junction leakage control is studied with electron beam (e-beam) defect inspection after tungsten chemical mechanical polishing (WCMP). Leakage-induced bright voltage contrast (BVC) defects are detected. For both wafer to wafer (WtW) and within wafer (WiW), e-beam inspection results strongly correlate with leakage results of wafer acceptance test (WAT). Failure analysis results showed that the junction leakage was caused by lateral diffusion of nickel silicide (NiSi) underneath the spacer. The extrusion length correlates with gray levels of the tungsten plug very well. In this study we found the optimized condition to suppress junction leakage and also confirmed that post WCMP e-beam inspection can be used to monitor and control junction leakage.

INTRODUCTION

Introduction to e-beam defect inspection

Scanning electron microscope (SEM) has been increasingly used for defect inspection in IC chip fabrication because of the reduction of the killer defect dimension that comes along with the shrinking of the device geometry. Besides detecting the physical defects that are beyond the capability of optical inspection equipment, the unique capability for e-beam to detect electrical defects such as circuit shorts or leaks and open or partially open circuits make it an equipment of choice for interconnect process inspection and monitoring. [1], [2], [3]

Figure 1 illustrates eScan®300, which is an e-beam inspection system developed by Hermes Microvision Incorporated (HMI). Its e-beam system consists an electron gun, an e-beam column, objective apertures, a ring-shaped semiconductor detector to detect both secondary electrons (SE) and back scattered electrons (BSE), and a focus lens assembly. [4]

When the electrons in the primary beam hit a tiny spot (a pixel from 30 to 100 nm) on the wafer surface, they will excite many SE and BSE, as well as some other electrons and photons out of that

Metrology, Inspection, and Process Control for Microlithography XX, edited by Chas N. Archie, Proc. of SPIE Vol. 6152, 615249, (2006) · 0277-786X/06/$15 doi: 10.1117/12.656207

surface. The brightness or the gray level value (GLV) of the pixel in the SEM image is determined by the total number of electrons from this pixel that are collected by the detector.

SEM images with 6144 by 6144 pixels can be formed at the same sampled locations of different dies. By comparing the GLV difference of the pixels of the images in different dies, we can detect defects on product wafers for non-destructive, in-line process monitoring.

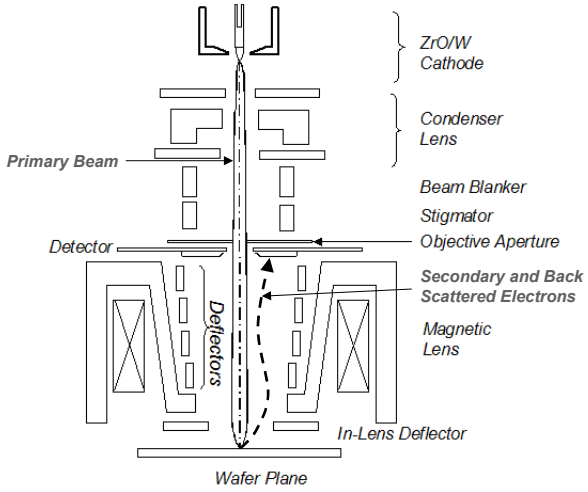


Figure 1. Schematics of the e-beam system of eScan®300.

The landing energy (LE) of 250 to 2500eV of the primary electron beam can be controlled by the total bias between electron gun and wafer. The relationship of LE and yield rate of the SE, BSE and their combinations are shown in Figure 2. [5] We can see that when E_1<LE<E_2, more electrons leave the surface than that reaches it, thus inducing a positive charge on the surface. Inspections described in this paper are performed in this regime, which is called "positive model".

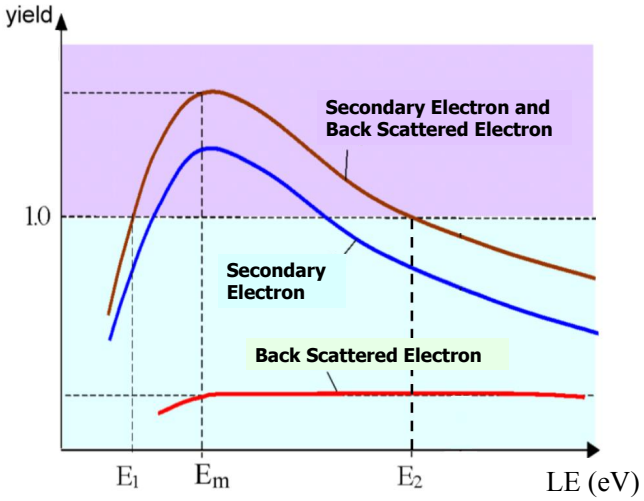


Figure 2. Relationship of LE of primary beam and SE and BSE yields.

Post-WCMP e-beam inspection

The chemical vapor deposition (CVD) process is commonly used to deposit tungsten (W) to fill the narrow contact holes that form conducting plugs to connect metal lines to silicide on active areas of silicon such as source/drain and polysilicon gate electrodes. There are several different connections of tungsten plugs (W-plugs) in complementary metal-oxide-semiconductor (CMOS) logic device, such as: a) P+/N-well, b) N+/P-well, c) short polysilicon gate, d) long polysilicon line, e) P+/P-well and f) N+/N-well. Because the different electrical properties of these structures, the voltage contrast (VC) of W-plugs in a SEM image is quite different and can be used to detect electrical defects such as short (leak) and open defects.

Figure 3 shows the surface charge situation and the expected VC of the SEM image of W-plugs with different connections at positive mode. At positive mode, the W surface tends to charge positively. Positive charges quickly build up to form a positive surface potential for W-plugs that contact to the short polysilicon gate and N+/P-well junction and prevents SE with low kinetic energy to leave the surface and get collected by the detector. Therefore, their SEM images look darker than the normally bright W-plugs that contact to P+/N-well, N+/N-well, P+/P-well and long polysilicon lines. For these normally bright W-plugs, positive charges can't build up during the e-beam scan because electrons from the silicon substrate or long polysilicon line can quickly neutralize the surface and allow more SE be collected by the detector.

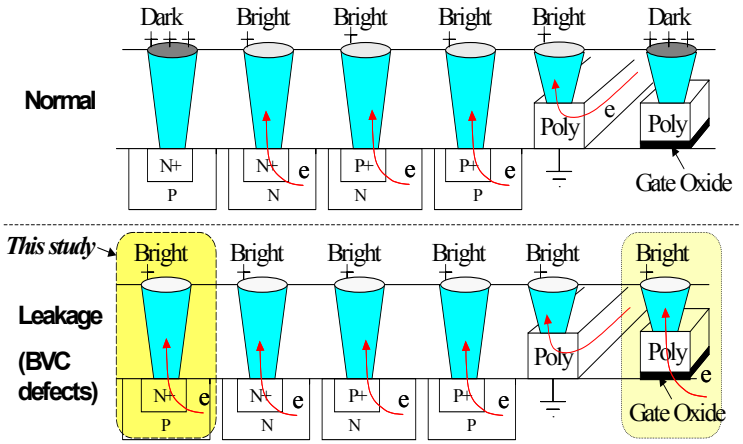


Figure 3. W-plug VCs with different connections in positive mode.

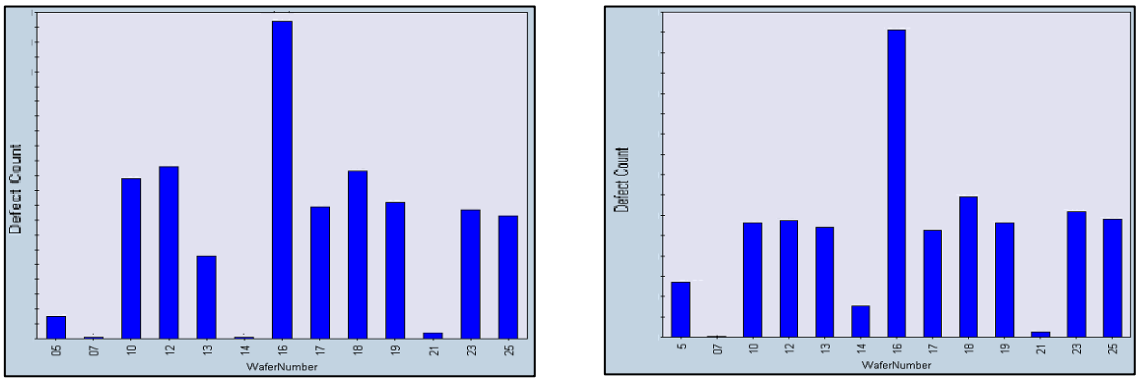
If the W-plug contacts with a leaky junction or a polysilicon gate with leaky gate dielectric, electrons from the substrate can neutralize the positive charges, therefore, its SEM image looks brighter than normal. The contrast is especially high for normally dark plugs, such as plugs that connect to N+/P-well or short polysilicon gate. It is commonly called bright VC or the BVC defect.

The GLV of the W-plug is related to the severity of the leakage; the more severe of the junction leakage, the higher the GLV.

EXPERIMENTS

Thirteen wafers with three split conditions are used in the experiment. After WCMP, wafers are inspected by eScan® 300 and BVC defects are found on the two test keys. Wafers then continue to process until metal 1 copper CMP (M1 CuCMP) for electrical test (also called WAT).

BVC defect counts of test key 1 and test key 2 for the 13 wafers are illustrated in Figure 4a and 4b, respectively. Leakage currents are measured after M1 CuCMP, as shown in Figure 5. Strong correlations are observed between leakage current and both BVC counts of test key 1 and test key 2, as illustrated in Figure 6.



(a) (b)

Figure 4. Total BVC defect counts of the thirteen wafers (a) on test key 1, (b) on test key 2.

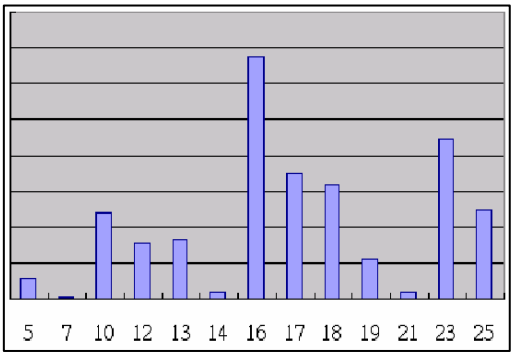


Figure 5. WAT leakage current of the thirteen wafers.

In another experiment, six wafers with three process splits are used in this experiment. Each split represents a different ion implantation process condition. After WCMP, one wafer from each split is sent to eScan® 300 for inspection and the rest continue processing until M1 CuCMP for electrical test.

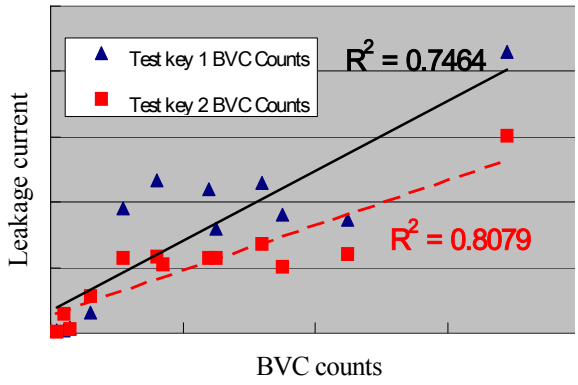


Figure 6. Correlations between WAT leakage current and the total defect counts of the test key 1 and test key 2.

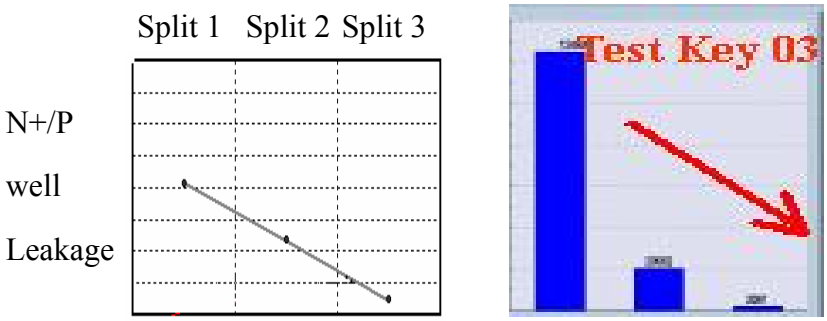
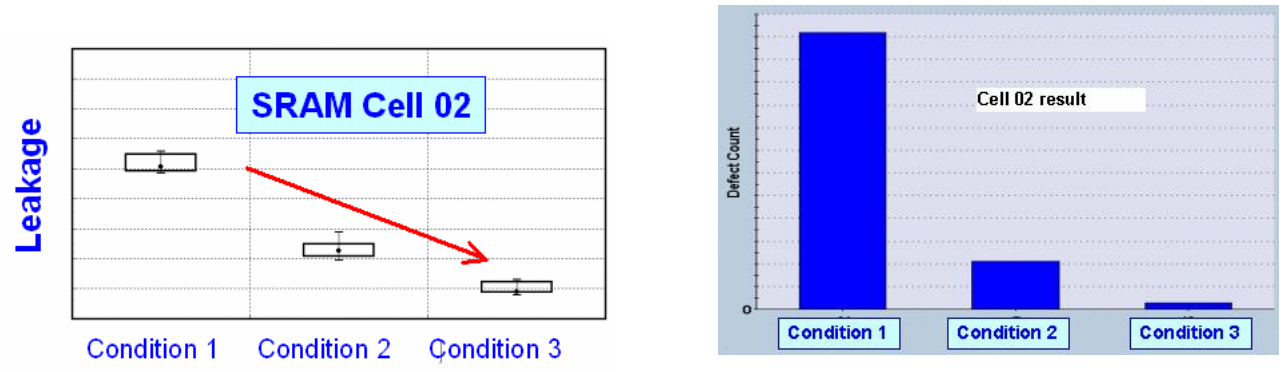


Figure 7. WAT leakage currents (a) and BVC defect counts of eScan®300 (b) on test key 3 at three process conditions

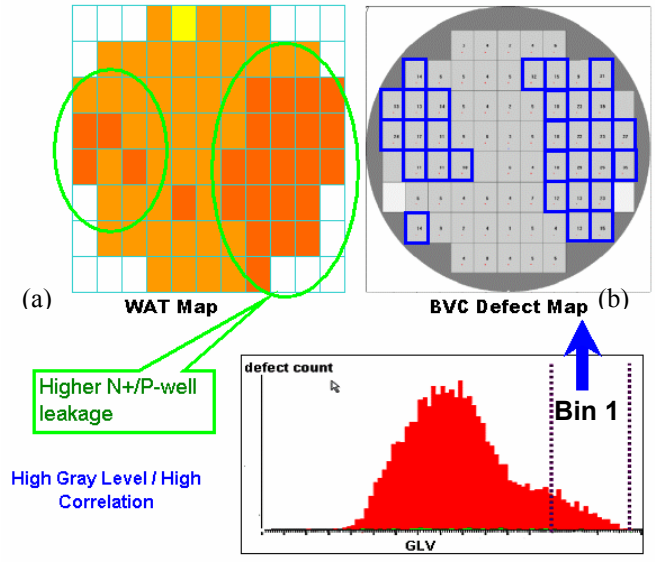
Die-to-die e-beam inspection at positive mode is performed on a WCMP wafer. BVC defects of W-plugs on N+/P-well junctions are analyzed by the binning of different GLV. We've found that the wafer with a process condition that has a high WAT leakage current also has a high BVC defect count, and their results correlate well on both test key and in the SRAM cell, as show in Figure 7 and Figure 8. Figure 7a shows the leakage current on test key 3 in three different process conditions and Figure 7b is the BVC defect count on test key 3 for the three process splits. Figure 8a shows the leakage current on the SRAM cell in three different process conditions, while Figure 8b shows the BVC defect counts on SRAM cell. Test key WAT leakage shown in Figure 9a matches GLV Bin 1

(high GLV) BVC defect maps shown in Figure 9b very well. Figure 9c is the histogram of the GLV for BVC defects; BVC with high GLV are grouped in Bin 1. Figure 10 (a), (b), (c) and (d) are eScan® review images of W-plugs of BVC defects with GLV1, GLV2, GLV3 and GLV4, respectively. Burn marks were created after taking the review images so these defects can be easily re-captured in failure analysis lab.



(a) (b)

Figure 8. WAT leakage current (a) and BVC defect counts (b) on SRAM cell at three process conditions.



(c)

Figure 9. WAT leakage current map (a), high GLV BVC defect maps (b) and histogram of GLV of BVC defects (c).

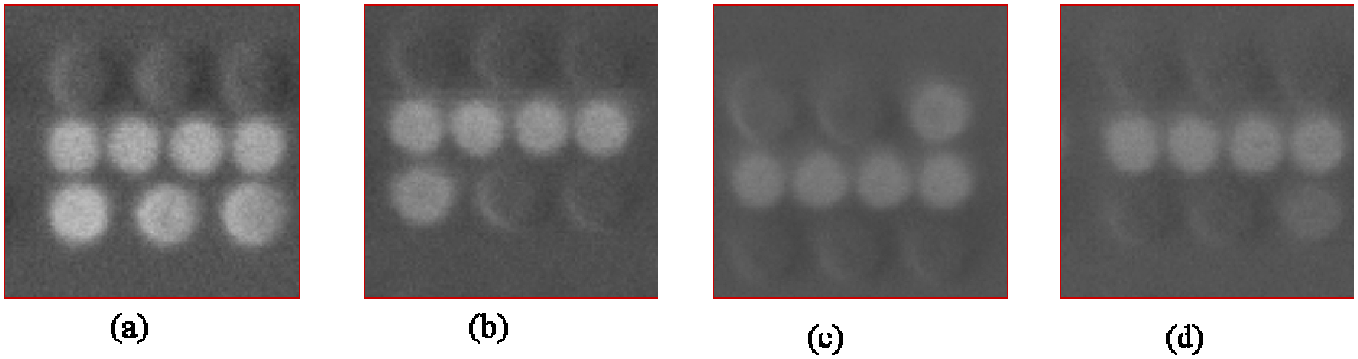
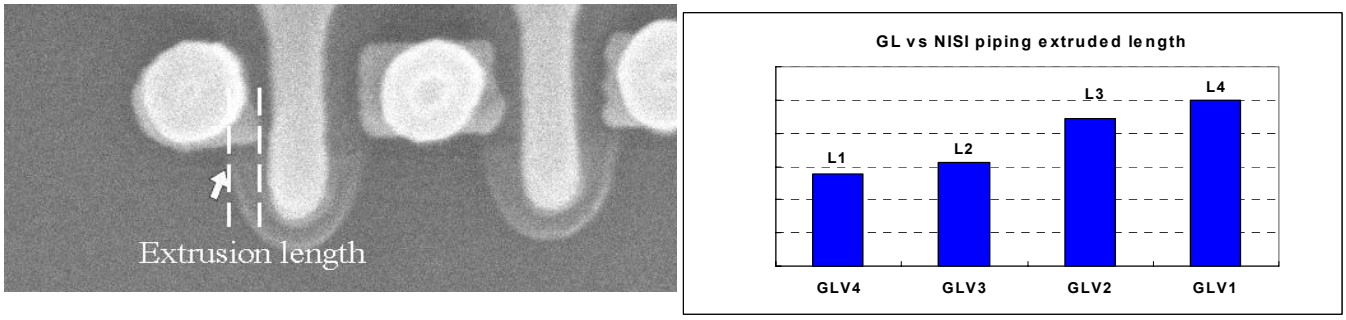


Figure 10. eScan®300 review images after ILD and spacer strip. BVC W-plugs with GLV1 (a), GLV2 (b), GLV3 (c), and GLV4 (d).

After the delayer of interlayer dielectric and sidewall spacer nitride in the failure analysis lab, review of the SEM image revealed that the N+/P-well leakage is caused by the lateral diffusion of nickel silicide underneath the spacer. It is also called NiSi piping defect of which, as shown in Figure 11a, are the W-plugs with GLV1. The extrusion length of the Ni diffusion is almost linearly correlated with the GLV of the eScan®300, as illustrated in Figure 11b. Cross-section SEM and TEM images in Figure 12a and 12b illustrate the detail of nickel silicide diffusion underneath the surface, which causes the junction leakage.



(a) (b)

Figure 11. (a) Review SEM image of GLV1 W-plug after ILD and spacer strip, (b) Correlation of BVC GLV and NiSi extrusion length.

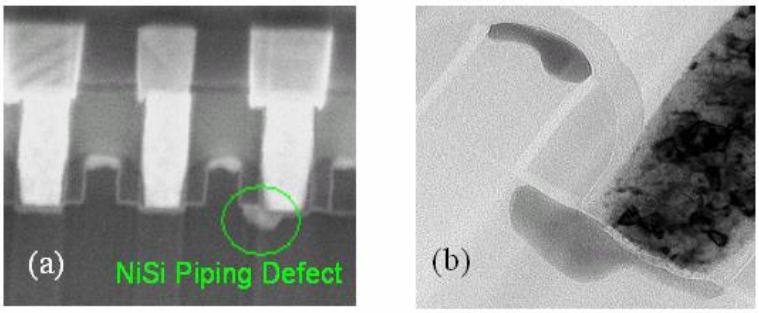


Figure 12. Images of nickel silicide lateral diffusion by cross-section SEM (a) and by TEM (b).

CONCLUSION

In this study, post-WCMP e-beam inspection has been used to detect BVC defects of W-plugs that connect to NiSi on the N+/P-well junction on test key structures and SRAM arrays to determine the optimized process condition to suppress NiSi diffusion induced junction leakage. WAT leakage current data correlate with BVC defect counts very well for both WtW and WiW. Similar die map signatures are found for both WAT leakage current and high GLV (Bin 1) BVC defects. Failure analysis results reveal that the junction leakage is caused by lateral diffusion of nickel silicide underneath the spacer and the extrusion length of the nickel silicide strongly correlates with GLV of the W-plug in close inspection of the SEM image.

Therefore, we can monitor N+/P-well junction leakage caused by lateral diffusion of nickel silicide by detecting N+/P-well W-plug BVC defects with BVC defects and GLV binning during in-line post-WCMP e-beam inspection.

ACKNOWLEDGEMENT

Special thanks to Wei Fang, Yu-Tsorng Fu, and Pang-Chi Mao of Hermes Microvision Inc. for their supports.

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