Investigation and solution of bump-like killer defects

YE-O-135

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Abstract – In this study, we investigated the root cause of the conducting bump defects detected by optical inspection system that had the same signature as sampling pattern of electron beam inspection (EBI) at tungsten (W) chemical mechanical polish (CMP) and at copper (Cu) CMP. We found that the bump defects were formed due to the combined effects of EBI and de-ionized (DI) water clean right after EBI. Model of micro plating was proposed and experiment results agreed with the model. We also propose the solution to avoid the yield killing bump defects in future EBI applications.

INTRODUCTION

EBI is increasingly used in integrate circuit (IC) chip manufacturing process to capture both tiny physical defects that beyond capability of optical inspection system and electrical defects such as open and short beneath conducting plugs as voltage contrast (VC) defects. Because scanning electron microscope (SEM) scans electrons in serial nature and the amount of electrons that carry the information form each pixel is very limited, EBI is significantly slower than the optical inspection systems that use much larger amount of photons to carry inspection information. Therefore, most people use EBI systems in the sampled care areas of sampled dies and mainly apply EBI systems to capture and monitor VC defects. WCMP and CuCMP are among the commonly used layers of EBI applications to monitoring VC defects such as contact open and leak/short. [1], [2], [3]

DESCRIPTION OF THE PROBLEMS

Bump-like defects were observed by dark field (DF) optical inspection system at silicon nitride (SiN) cap layer after CuCMP, as shown in Figure 1a. Cross-section SEM image in Figure 1b showed the bump was underneath the SiN cap layer. Energy dispersive spectrometry (EDS or EDX) results shown in Figure 1c indicated the bump defects mainly consisted with Cu, which is conductive and could cause electrical short. Strong correlation between EBI die sampling map and DF bump defect map was observed, as shown in Figure 2a and Figure 2b. Figure 2c is the within die care area of eScan®300 inspection and Figure 2d shows the DF within die defect distribution, which also strongly correlated with each other.

Similarly, bump defects were also captured by DF inspection system at SiN cap layer after WCMP. WCMP bump defect review SEM image was shown in Figure 3a. EBI captured bump-induced electrical short at metal 1 (M1) CMP as round-shaped cluster bright VC (BVC) defects, indicated the WCMP bumps were also electrically conductive. Figure 3b is the EBI reference image of the Figure 3c is the EBI defect patch image. Figure 4a is review SEM image of bump defect captured by DF inspection after de-ionized (DI) water clean of a WCMP wafer that was just inspected by an EBI system. Figure 4b showed the EDX data of the defect in Figure 4a, which indicated that the bump formed after WCMP EBI mainly consists with W, similar to the bump formed after CuCMP that mainly consisted with Cu.

ANALYSIS AND EXPLANATION

Because bump defects are yield killers, we did thorough investigations to find the root cause. Since we did not observe bump defects in previous lots, we suspected the process change was the root cause. We checked the process flow and found that a DI water clean step was added between EBI and SiN cap layer deposition, as shown in Figure 5. The original purpose of the DI water clean was to remove possible particles before the SiN cap layer deposition. It gave us a hint that it was likely the combined effects of EBI and DI water clean caused the bump defects. Several theories were brainstormed and eventually we agreed on with the micro-plating model, as illustrated in Figure 6.

When energetic electron beam (e-beam) of EBI system scanned across the sample surface with both metal and dielectric, such as WCMP wafer or CuCMP wafer, it would breakdown the chemical bonds on metal surface, which made the metal easier to be oxidized when exposed to air and moisture. During DI water clean, excessive metal oxide, such as tungsten oxide formed due to e-beam bombardment of W surface dissolved in DI water as positive W^{+} ions, which quickly deposited on the dielectric surface to form bump-like defects and caused electrical short between W plugs. DI water clean right after CuCMP EBI can also from bump-like defect caused by deposition of Cu^{++} ions on the wafer surface.

EXPERIMENTS AND RESULTS

We used an EBI system, eScan®300, for the first two experiments with two WCMP wafers. Figure 7 illustrated the experiment steps of Experiment 1 with WCMP wafer #1 and the results shown in Figure 8. The purpose of the experiment was to determine whether WCMP EBI alone could generate bump defects. The first DF inspection (DF1) took after WCMP captured 448 defects, the second DF inspection (DF2) after DI water wafer clean captured 469 defects. The third DF inspection (DF3) after EBI captured 413 defects. None of these defects was bump-like defect. The results showed that EBI alone did not create the bump defects.

Figure 9 showed the process steps of Experiment 2 with WCMP wafer #2 to determine whether DI water clean after EBI was responsible to the bump-like residues. The results in Figure 10 showed the dramatic increase of defect count, 12456, captured by DF3 after DI water clean, comparing with the defect count of 577 captured by DF2 after EBI. Review SEM image showed most of the defect captured in DF3 were bump-like defects. That support our theory that micro-plating

due to by DI water clean immediately followed WCMP EBI formed the bump defects. Figure 11a and 11b are the review SEM images of the bump defects captured by DF3 of Experiment 2 near the wafer center and near the wafer edge, respectively.

In experiment 3, we used a review SEM system and WCMP wafer #3. Figure 12 showed the process flow of Experiment 3. DF1 before taking review SEM images found 70 defects, as shown in Figure 13a. DF2 after review SEM e-beam scan before DI wafer clean found 76 defects. DF3 found defect count sharply increased to 213 after DI water clean, as shown in Figure 13b. The review SEM images showed in Figure 14 clearly indicated the added defects were bump-like residues. We could see that if one did DI water clean on a WCMP wafer after taking review SEM images, it could generate bump defects. The results of experiments strongly supported the micro-plating model: it was the combination of e-beam scan and DI water clean of metal (W and Cu) CMP wafer that caused the conductive bump defects.

CONCLUSION

We found that the EBI alone would not create yield killing bump defects. The conducting bump defects were form only when DI water clean is performed right after EBI of WCMP wafer or CuCMP wafer. Defect formation mechanism was proposed and experiment results collected in this study strongly support our explanation. To avoid yield loss due the bump defects, one should perform DI wafer clean before EBI, not after it.

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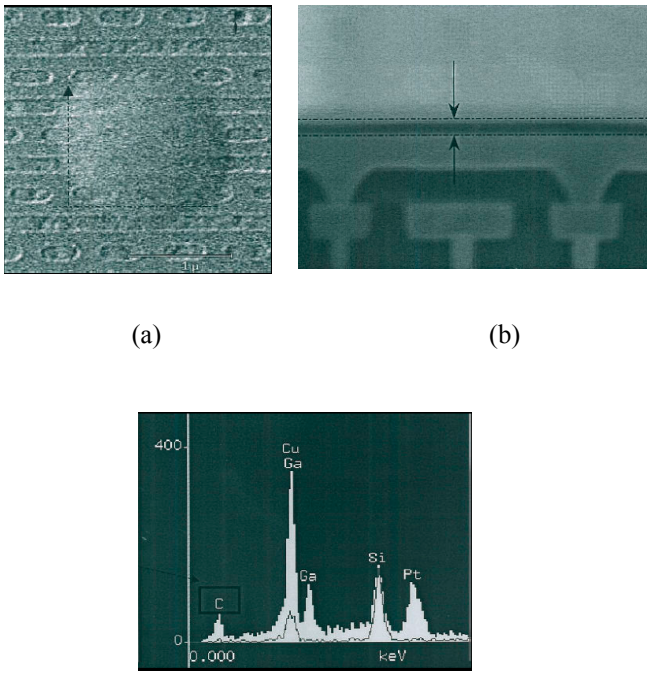
AUTHOR BIOGRAPHY

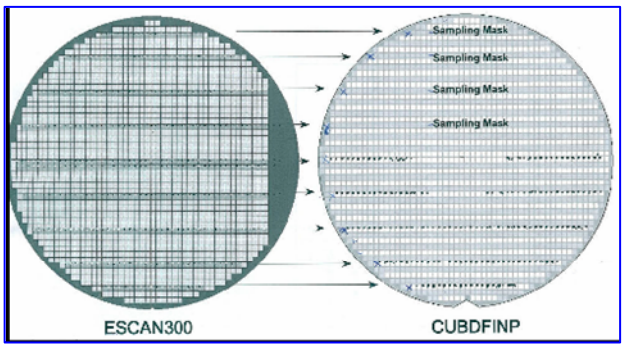
Hong Xiao, Ph.D., is a technical marketing specialist in Hermes Microvision, Inc. (HMI). He has over 10 year experience in semiconductor industry. Before join HMI, he was a senior process engineer in defect metrology group of Dan Noble Center of Motorola. Prior of that, he was an associate professor in Semiconductor Manufacturing Technology program of Austin Community College, and a senior technical instructor of technical training department of Applied Materials, Inc. He has 6 US patent applications pending and more than 20 publications in technical journals and conference proceedings. He is the author of the textbook "*Introduction to Semiconductor Manufacturing Technology*" published by Prentice Hall.



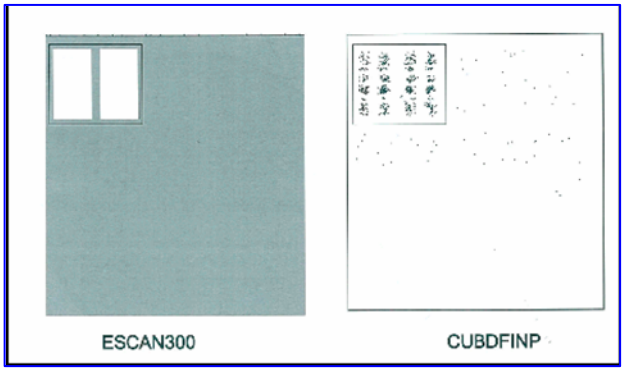
(a) (b)

(c)

Figure 1. (a) Review SEM image of bump defect on nitride cap of CuCMP, (b) cross-section SEM image of the bump defect, and (c) EDX data of the Cu CMP bump,

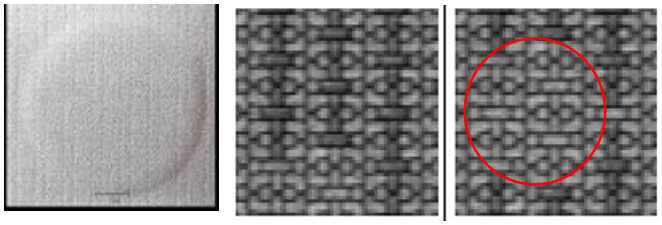


(a) (b)



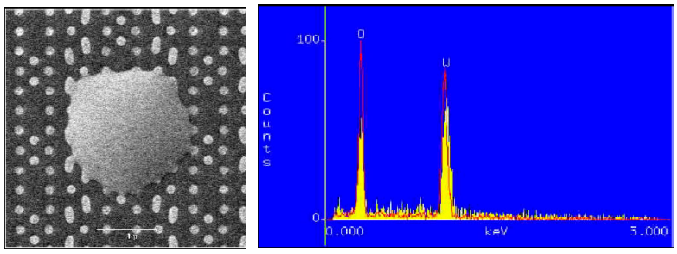
(c) (d)

Figure 2. (a) EBI die sample map, (b) DF defect map, (c) EBI care area within a die, and (d) DF defect distribution within a die.



(a) (b) (c)

Figure 3. (a) SEM review image of bump defect on nitride cap after WCMP, (b) reference image of M1 (c) cluster BVC detect patch image of M1.



(a) (b)

Figure 4. (a) Review SEM image of a bump defect of WCMP, (b) EDX data of WCMP bump.

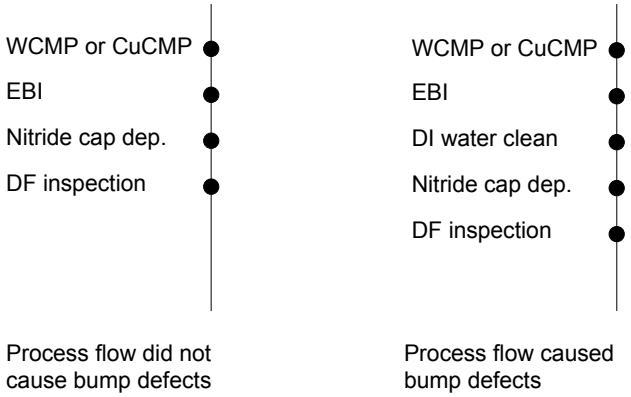


Figure 5. Process flows that caused bump defects and did not cause bump defects

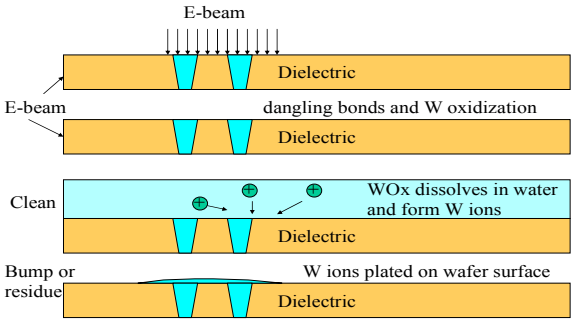
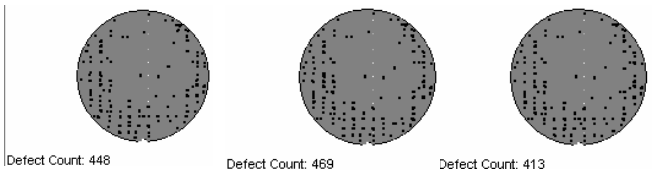


Figure 6. Illustration of WCMP bump formation.

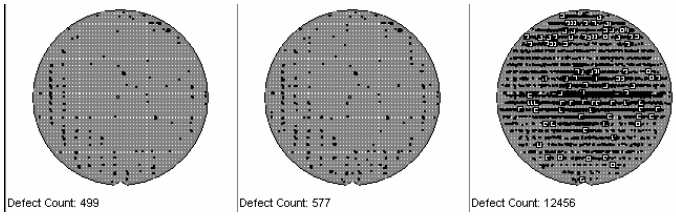
Figure 7. Process sequence of Experiment 1.



(a) (b) (c)

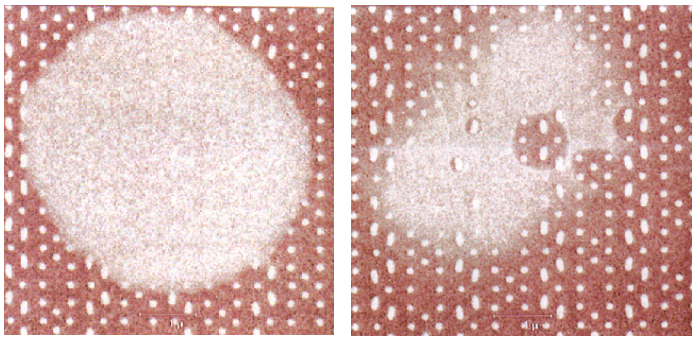
Figure 8. DF inspection defect maps of Experiment 1, (a) DF1, (b) DF2 and (c) DF3.

Figure 9. Process sequence of Experiment 2.



(a) (b) (c)

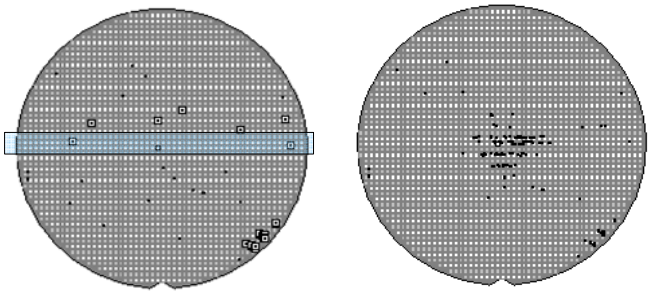
Figure 10. DF inspection defect maps of Experiment 2, (a) DF1, (b) DF2 and (c) DF3.



(a) (b)

Figure 11. Review SEM images of bump-like residue captured by DF3 of Figure10c. (a) Near wafer center and (b) Near the wafer edge.

Figure 12. Process sequence of Experiment 3.



(a) (b)

Figure 13. DF inspection defect maps of Experiment 3, (a) DF1 and (b) DF3.

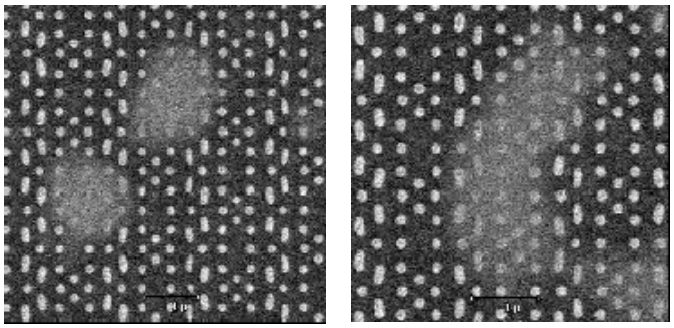


Figure 14. Review SEM image of bump-like residue captured in DF3 of Experiment 3.