Inspection and repair for imprint lithography at 32nm and below

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Abstract

Step and Flash Imprint involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed leaving a patterned solid on the substrate. Compatibility with existing CMOS processes requires a mask infrastructure in which resolution, inspection and repair are all addressed. The purpose of this paper is to understand the progress made in inspection and repair of 1X imprint masks

A 32 nm programmed defect mask was fabricated. Patterns included in the mask consisted of an SRAM Metal 1 cell, dense lines, and dense arrays of pillars. Programmed defect sizes started at 4 nm and increased to 48 nm in increments of 4 nm. These defects were then inspected using three different electron beam inspection systems. Defect sizes as small as 8 nm were detected, and detection limits were found to be a function of defect type. Both subtractive and additive repairs were attempted on SRAM Metal 1 cells. Repairs as small as 32nm were demonstrated, and the repair process was successfully tested for several hundreds of imprints.

Keywords: step and flash imprint lithography, S-FIL, imprint lithography, imprint mask, electron beam inspection, e-beam repair, mask repair

1. Introduction

Step and Flash Imprint Lithography redefines nanoimprinting.[1-3] This novel technique involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed leaving a patterned solid on the substrate. Recent publications have highlighted resolution and overlay[4,5]: Variable shape beam systems are now providing mask resolution below to 32nm, and overlay numbers well below 20nm have been reported.

Compatibility with existing CMOS processes requires a complete mask infrastructure in which resolution, inspection and repair are all addressed. Previous work using a KLA-T optical inspection tool to directly inspect the 1X mask was successful in identifying many types of defects smaller than the actual pixel size (90 nm) used to inspect the mask.[6,7] The ITRS roadmap calls for detection of 20nm defects at a 22nm half pitch in 2013 and 10nm defects for a 20nm half pitch in 2015. The purpose of this paper is to understand the limitations of inspection and repair at half pitches of 32 nm and below.

An inspection test mask was designed, and included dense features (with half pitches ranging between 32 nm and 48 nm) containing an extensive array of programmed defects. The mask was used to imprint 300mm wafers, and the printed defect arrays were examined using electron beam inspection tools. Both die-to-die and die-to-database inspections were performed. A similar mask was designed to examine the feasibility for doing both subtractive and additive repairs on a fused silica imprint mask.

2. Experimental Details

To generate the inspection test mask, patterns were exposed by Dai Nippon Printing using a JEOL 9300 Gaussian beam pattern generator. ZEP520A resist was chosen as the positive imaging resist. After development, the chromium and fused silica were etched using Cl_2/O_2 and fluorine-based chemistry, respectively. Mesa lithography and a mesa etch process, followed by a dice and polish step were employed to create a finished 65 mm x 65 mm template.[8]

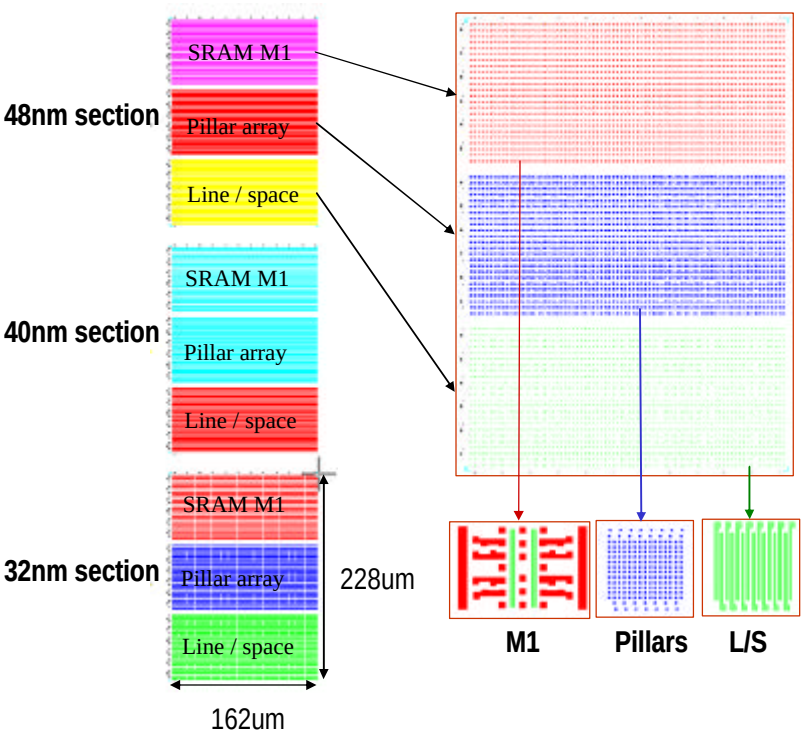

Figure 1. Programmed defect layout

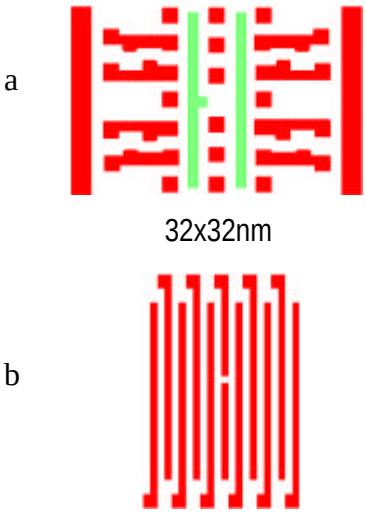

Figure 2. a) Extension defect in the SRAM Metal1 pattern. b) Mousebite in the line/space array.

The pattern chosen for evaluation was a 32 nm half pitch design with several different pattern types. Each pattern, in turn, had an array of programmed defects introduced into the pattern. The details are shown in Figure 1. Three different half pitches were studied: 48 nm, 40 nm and 32 nm. For each size, three pattern types were designed: SRAM Metal 1, pillar array, and a dense line/space pattern. For each feature type, multiple programmed defects were inserted. As an example for the 32nm lines and spaces, twelve incremental programmed sizes were inserted, starting at 4 nm and ending at 48 nm. Extension defects included three repeats in the horizontal and vertical directions , for a total of 72 defects. Mousebites were inserted in the same fashion to create a total of 144 defects. Examples of extension defects for the Metal1 and mousebites in the line/space pattern are shown in Figure 2.

A similar mask was used to do the initial repair evaluation. In this case, 1 100nm Metal 1 cell was embedded with programmed defects. Defect types included mousebites, extensions, shrinking pillars and line shortening.

Initial characterization of the imprint mask was done using both a Holon EMU-270A SEM and a KLA-Tencor LWM9045 SEM. The EMU-270A is capable of 1.5 nm resolution at 1.0 kV when applying aberration correction. Low vacuum operation, combined with proprietary charge control enables high quality imaging on uncoated fused silica masks. The KLA-Tencor LWM9045 CD SEM uses proprietary technology to control the charging effect, employs a new electron detector system, and provides stable imaging conditions to avoid image drift.

Imprinting of the mask pattern was performed by using a Molecular Imprints Imprio® 300 imprint tool. A Drop-On-Demand method was employed to dispense the photo-polymerizable acrylate based imprint solution in field locations across a 300 mm silicon wafer. The template was then lowered into liquid-contact with the substrate, displacing the solution and filling the imprint field. UV irradiation through the backside of the template cured the acrylate monomer. The process was then repeated to completely populate the substrate. Details of the imprint process have previously been reported.[9]

Critical dimension (CD) images of the imprinted patterns were captured with a JEOL JSM-6340F field emission cold cathode SEM equipped with a tungsten emitter. The accelerating voltage can be varied from 0.5 to 30 kV. The system has intrinsic 1.2 nm resolution capability at 15 kV accelerating voltage, and 2.5nm at 1 kV. CD measurements and line width roughness data were then extracted offline using the SIMAGIS® automated image metrology software suite from Smart Imaging Technologies.[10]

Die-to-die wafer inspection was done with both a KLA-Tencor eS35 and a Hermes Microvision (HMI) eScan 315 electron beam inspection . The eS35 operated at a data rate of 50 megapixels per second, with pixel settings of 15, 20, and 25nm. Landing energy was set to 1750 volts and eight scans were collected. The eScan 315 operated at a data rate of 100 megapixels per second with pixel settings of 10 and 15nm. Landing energy was 2000 volts and eight scans were also collected. Die-to-database inspection was performed using an NGR2100 e-beam wafer system. The data rate was set at 50 megapixels per second, and the landing energy was 2600 volts. Although a 3nm pixel setting was used, the detection threshold was set to 10nm.

The repair experiments have been performed on a Zeiss MeRiT development tool, which utilizes e-beam induced etch and deposition processes. When a defect is located on the substrate, suitable precursor gases are dispensed in very close vicinity to the incident electron beam. Details on this process have been previously reported.[11, 12]

3. Results

a. Mask SEM inspection

Images of the programmed defects for all pattern types were captured with the Holon EMU-270A SEM. Examples of the 32 nm Metal 1 extension defects are shown in Figure 3. The 4 nm defect is difficult to discern. Starting at 8 nm, all of the programmed defects are visible.

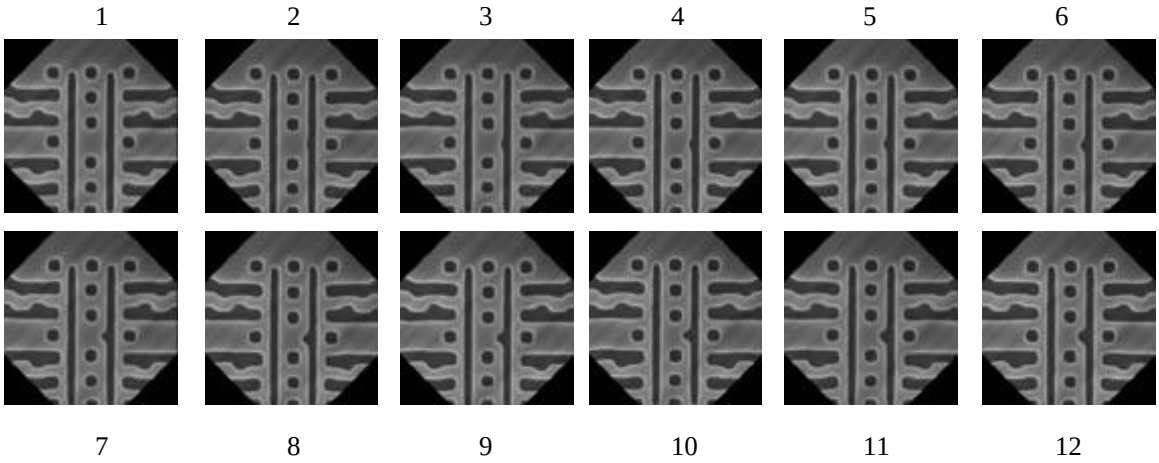

Figure 3. Programmed extension defects in the 32 nm Metal 1 pattern

A second set of images, taken with the KLA-Tencor LWM9045, is shown in Figure 4. In this case, mousebite defects were included in the line/space pattern. Once again it is difficult to discern the 4 nm programmed defect. Programmed defects from 8 nm up to 16 nm appear as defects along the edge of the line. At 20 nm (Image 5, top row), the defect causes the line to open, causing a non-linear behavior in the progression of the defective area.

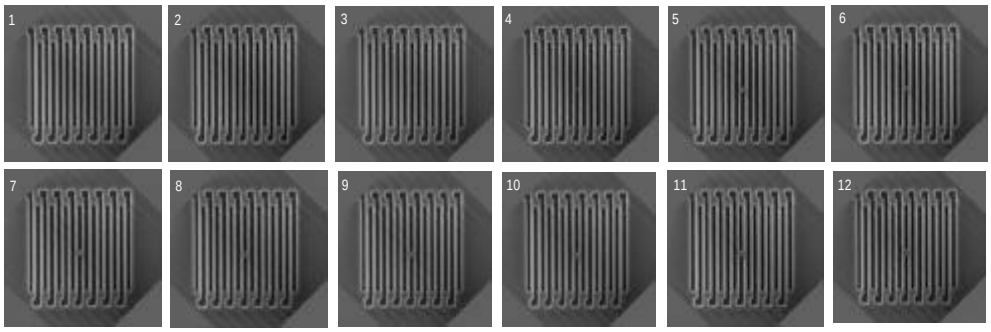

Figure 4. Mousebite defects in the line/space pattern

b. Imprint analysis

Following the imprinting on 300 mm silicon wafers, SEMs were again collected in the programmed defect areas in order to understand the correlation between the defects on the mask and the actual printed defects. Figure 5 depicts the programmed defects in the 32 nm Metal 1 patterns. Note that the location of the defect is mirrored in x relative to the mask images, because of the imprint process. Imprinted lines with the mousebite defects described earlier are shown in Figure 6. Again, note the nonlinear behavior in the actual programmed defect size.

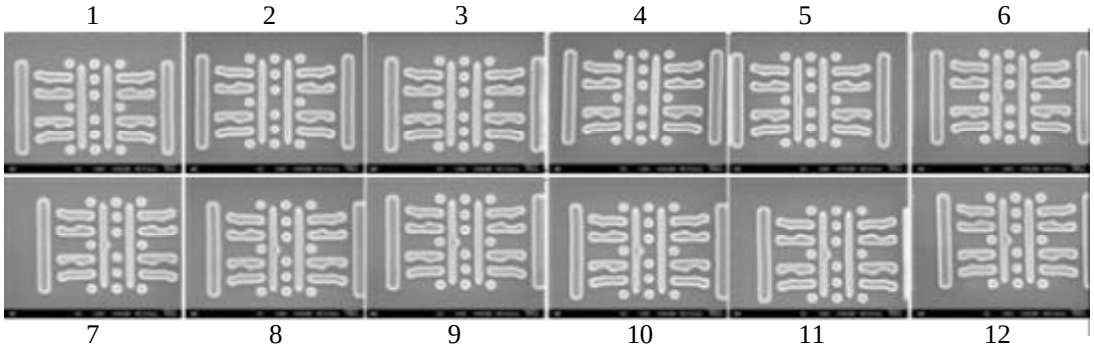

Figure 5. Programmed defects from the 32 nm Metal 1 pattern imprinted on to a 300 mm silicon wafer.

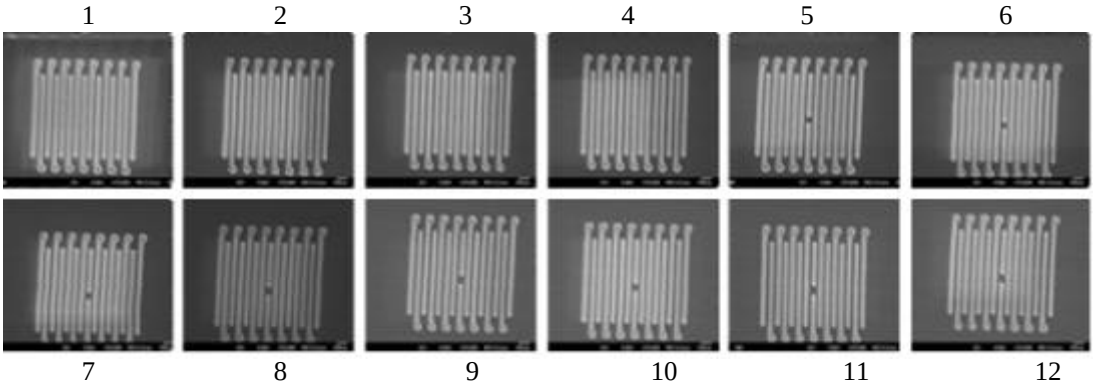

Figure 6. Programmed defects from the 32 nm line/space pattern imprinted on to a 300 mm silicon wafer.

SIMAGIS analysis software was used to calculate the actual defect area on the mask and on the imprinted wafer for each programmed defect as a function of the coded defect size. The defect area was obtained by taking the defect image, adjusting the image threshold, shifting the image by a single pitch, and then subtracting the shifted image from the original. The pixilated difference can then be converted into a defect area. An example of this technique is shown in Figure 7.

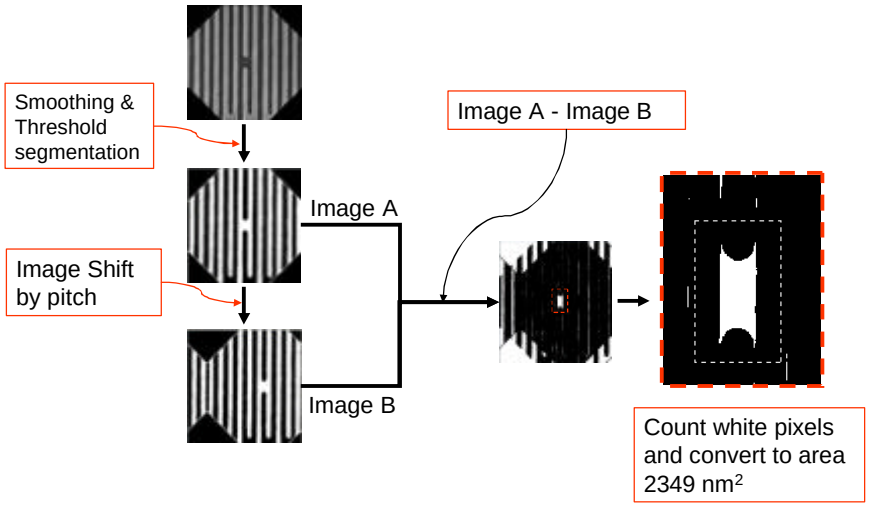

Figure 7. Determination of the actual defect area using SIMAGIS analysis software.

The defect size trend for both mask and imprint are shown in Figure 8. Pictured are the trends for the Metal 1 defects and the shrinking pillars. Both graphs show excellent agreement in defect size between the mask and imprint. As expected, the Metal 1 trend curve is linear. In comparison, a discontinuity (similar to that seen in the line/space pattern) is observed in the chart of the dense pillars. As the pillar is shrunk to a diameter less than 16 nm, the feature is no longer resolved on the mask, and the defective area jumps in size. The defective area then remains constant until the programmed pillar above the central pillar is also shrunk.

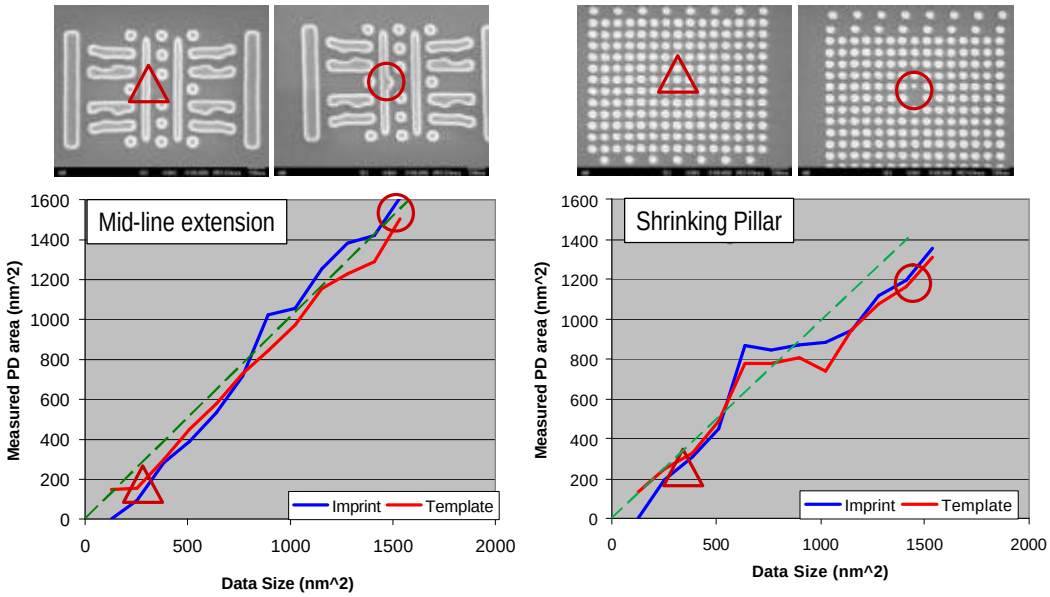

Figure 8. Measured defect size versus coded defect size for both the Metal 1 pattern and the dense pillar array.

c. eS35 Inspection Results

The eS35 wafer inspection system was used to observe the patterned defects. The system operated at a data rate of 50 megapixels per second, with a pixel settings of 15, 20, and 25 nm. Landing energy was set to 1750 volts and eight scans were collected.

The entire data set is shown in Figure 9. Plotted are the detected defects for all of the patterns and all of the defect sizes at three different pixel inspection settings. The majority of the 20 nm defects are detected (indicated on the graph for the 32 nm defects with an arrow), even at an eS35 pixel setting of 25 nm. As the pixel size is reduced to 15 nm, all of the 20 nm programmed defects are detected and a majority of the 16 nm defects are also captured.

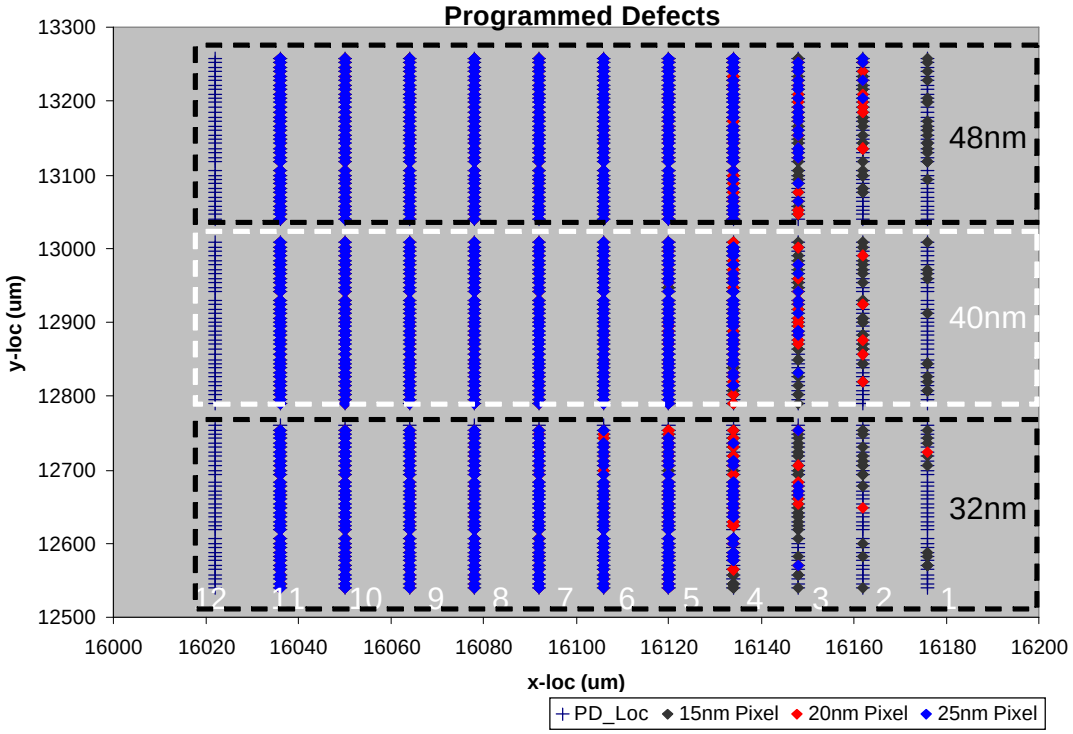

Figure 9. Programmed defect detection as a function of the pixel setting for all patterns

Details of the captured defects for the 32nm patterns are shown in Figure 10. Pictured is the capture rate of all of the various programmed defect types as a function of the coded defect size at two different pixel sizes. Two trends are clearly observed: 1) Pixel setting has a significant effect on defect detection. As the pixel size decreases from 25 nm to 15 nm, the minimum defect size observed decreases from 18 nm to 11 nm. 2) Minimum defect size is dependent on the programmed defect type. The eS35 was most sensitive to shrinking pillars and least sensitive to extensions in the Metal 1 pattern. These two particular trend lines are shown more clearly in Figure 11. Figure 11 depicts the capture rate as a function of the actual measured defect area and indicates a sensitivity in the shrinking pillar array and Metal 1 extension of 10 nm and 18 nm, respectively. These results align well with the ITRS requirements for NAND Flash at 22 nm.

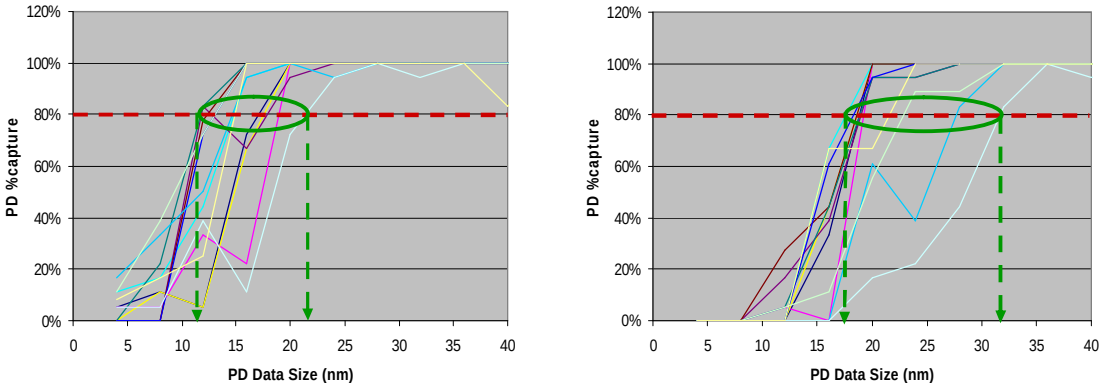

Figure 10. Capture rate as a function of data size for two different pixel settings (15nm left, 25nm right).

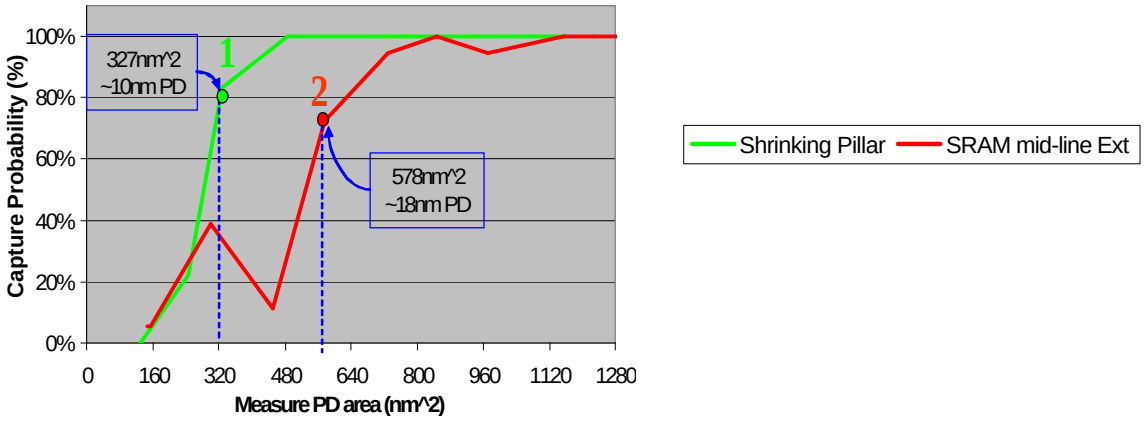

Figure 11. Capture rate as a function of the measured programmed defect area.

d. HMI eScan 315 Results

The 32nm programmed defect cells were examined at pixel settings of 10 and 15nm. The result of the inspection is shown in Figure 12. The blue dots in Figure 12 indicate the programmed defects captured at a 15nm pixel setting. All of the 16nm programmed defects were captured, and more than half of the 12nm defects were captured. As in the case of the results from the eS35, the eScan system is most sensitive to changes in the pillars. In fact, at a 15nm pixel setting, all of the 8nm programmed defects are captured. Better results are obtained at the 10nm pixel setting (red cells). All but one of the 12 nm defects are detected, and 67% of the 8nm defects were observed.

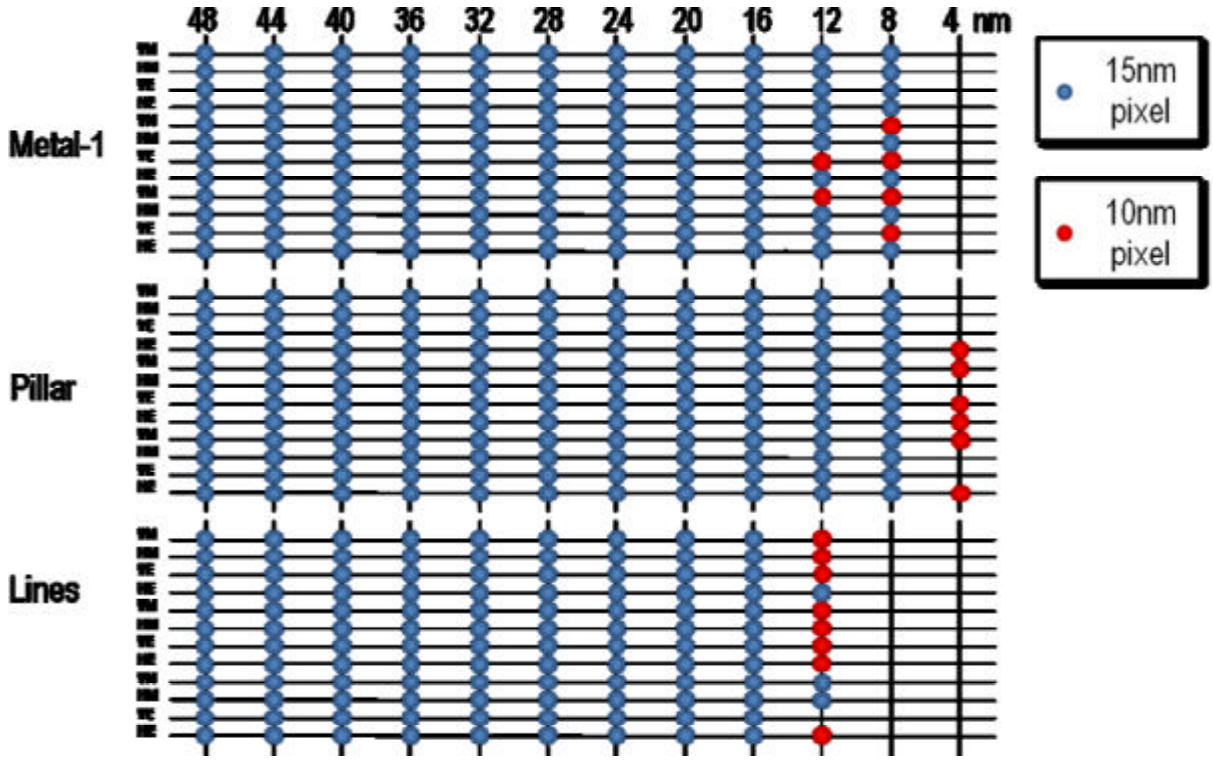

Figure 12. Captured programmed defect map for two pixel settings: 15nm (blue), 10nm (red).

The data indicates that the inspection system is most sensitive to pillar type defects and least sensitive the defects in the dense line patterns. It should be noted that visually, the 8nm programmed defects in the dense line patterns tend to be small relative to the coded defect size, so it is not surprising that the defects for these cells are more difficult to detect. The improvement in defect detection as the pixel setting is reduced from 15nm to 10nm is easily observed in Figure 13. 80% capture rates were compared for both pixel sizes. Capture size ranges between 7 and 15nm for the 15nm pixel, and drops to 6 to 12nm for the 10nm pixel. In both cases, best results are obtained for the pillar defects.

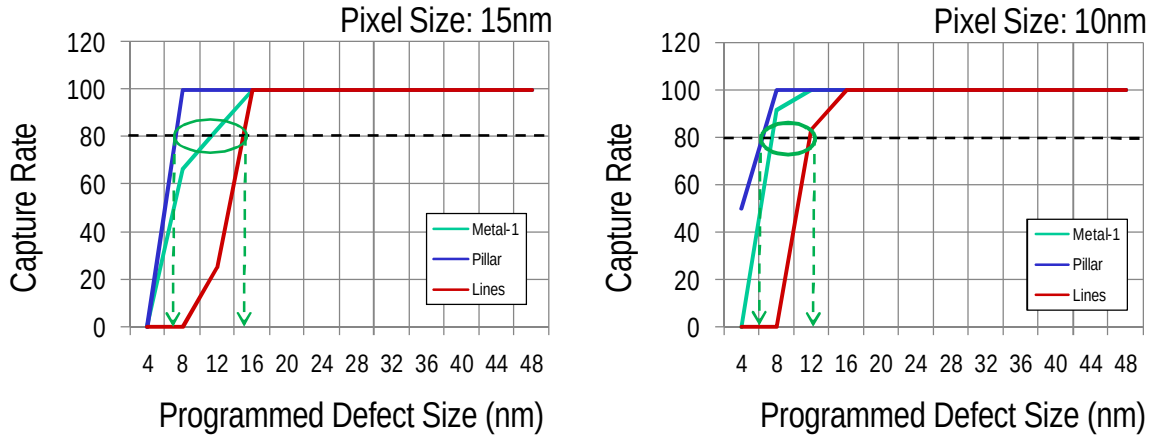

Figure 13. Capture rate as a function of programmed defect size for 15nm and 10nm pixel settings.

Figure 14 depicts several of the smallest defects captured with a 10nm pixel setting. It is also interesting to note that a few 4nm programmed defects were captured. Despite the minimal linewidth roughness on the mask used for this study (only 2.2nm, 3σ) it starts to become difficult to separate the signal from the defect from the edge noise of the reference features at 4nm.

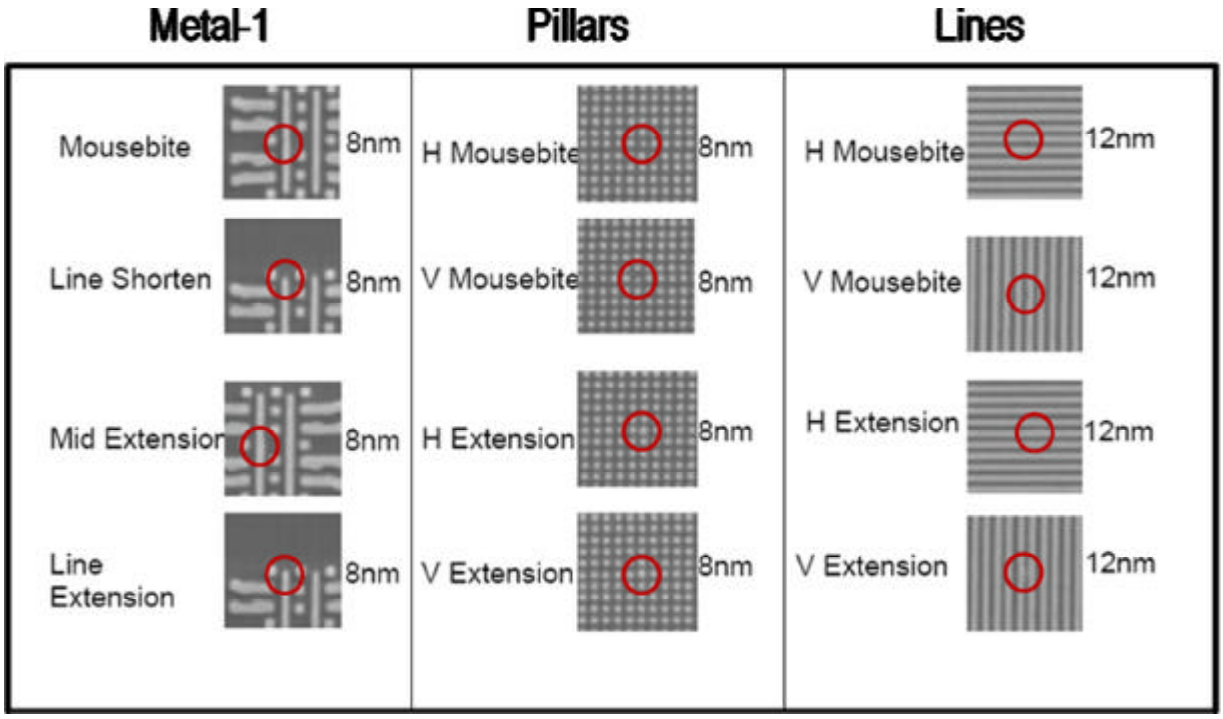

Figure 14. Scanned images of several of the smallest detected defects.

e. NGR2100 results

The NGR2100 was used to do a die-to-database inspection of the 32 nm dense line and Metal-1 patterns. The NGR2100 inspection consists essentially of a pixel by pixel scan of the critical pattern.[13] In this case, the detection threshold was set to 10 nm. Examples of the resolution of the system are shown in Figures 15 and 16. Shown in Figure 15 is a 16 nm line extension in the Metal-1 pattern. Figure 15a depicts the entire unit cell. Figure 15b shows a detailed view of the defect. Figure 16 shows comparable results for an 8nm mousebite in the line/space array.

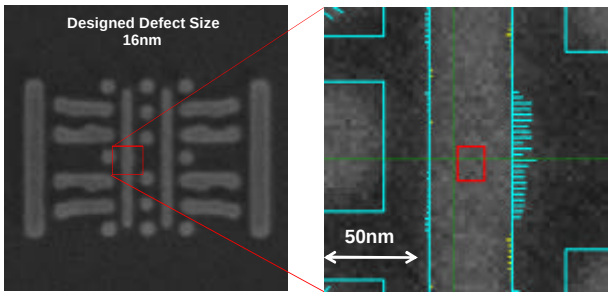

Figure 15. A 16nm extension defect in the Metal-1 cell.

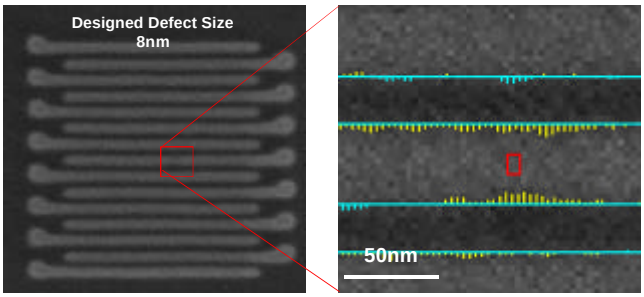

Figure 16. An 8nm mousebite in the 32nm line/space array.

It is interesting to note that once again the detection sensitivity was also impacted by the particular pattern and defect type. This effect is shown in Table 1. As in the case of the previous inspections, all of the programmed defects sized 20nm and above were detected. Best sensitivity was noted for the mousebite defects in the dense line patterns.

Target Defect Size		48nm	....	20nm	16nm	12nm	8nm	4nm
Line	Horizontal	100%	100%	100%	100%	100%	33%	0%
Line	Vertical	100%	100%	100%	100%	100%	33%	33%
Space	Horizontal	100%	100%	100%	0%	0%	0%	0%
Space	Vertical	100%	100%	100%	67%	0%	0%	0%
M1 Mousebite		100%	100%	100%	100%	67%	0%	0%
M1 Extension		100%	100%	100%	33%	0%	0%	0%

Table 1. Defect inspection sensitivity for six different 32nm patterns.

f. Imprint Mask Repair

Electron beam repairs combine the energy of an incident electron beam with an appropriate precursor gas. Depending on the precursor chemistry, a reaction is induced by the focused electron beam. This leads to a deposition caused by fragmentation of precursor molecules or an etch reaction between the absorbed molecules and the substrate material, resulting in volatile products. Since the reaction is confined only to the area exposed by the electron beam, this technique allows high-resolution nanostructuring with resultant feature sizes well below 30nm. The repair structure is derived by comparing a high-resolution image of the defective area with the same image of a non-defective area. The repair shape is generated as the difference of these two images, and adjusted for processing purposes.

There are several requirements for the repair process when applied to imprint masks. Deposited material to repair opaque defects has to be transparent to UV light and has to exhibit good adhesion to the mask substrate. Otherwise material delamination can occur during the imprint process. One of the advantages of using e-beam for quartz removal is that etching can be made in small trenches with excellent profile control. On the other hand, the process has to be well adjusted to allow the removal of an accurate amount of material without removing surrounding material. This can cause a deviating geometry between the repaired and the reference structure.

Experiments with optimized repair tool parameters have been done with programmed defects fabricated on a $65\times65mm^2$ fused silica mask. Figure 17 shows SEM images of programmed clear defects consisting of a 2D extension, line-end shortening, shrinking contact and 2D mouse bite. Additionally, the mask pattern contains internal mouse bite defects. Figure 18 shows the same defect pattern after repair.

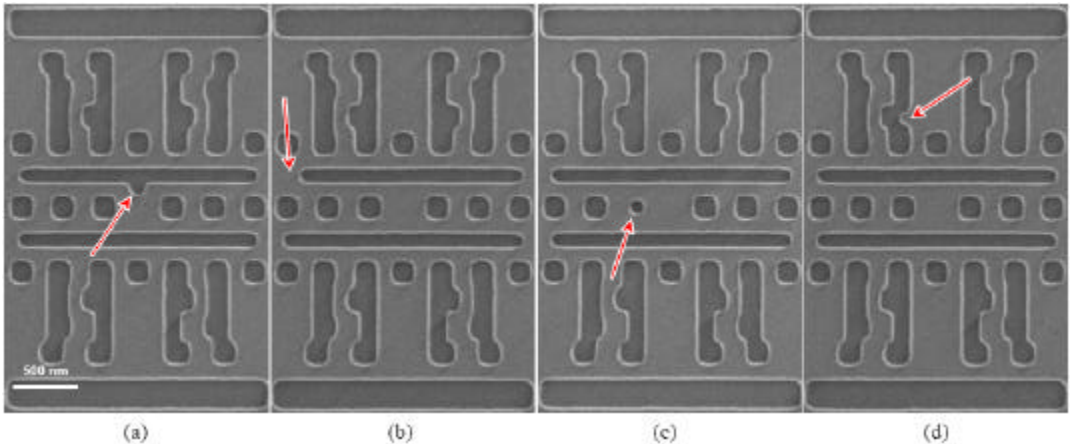

Figure 17. Programmed defects in a 100nm SRAM Metal 1 unit cell

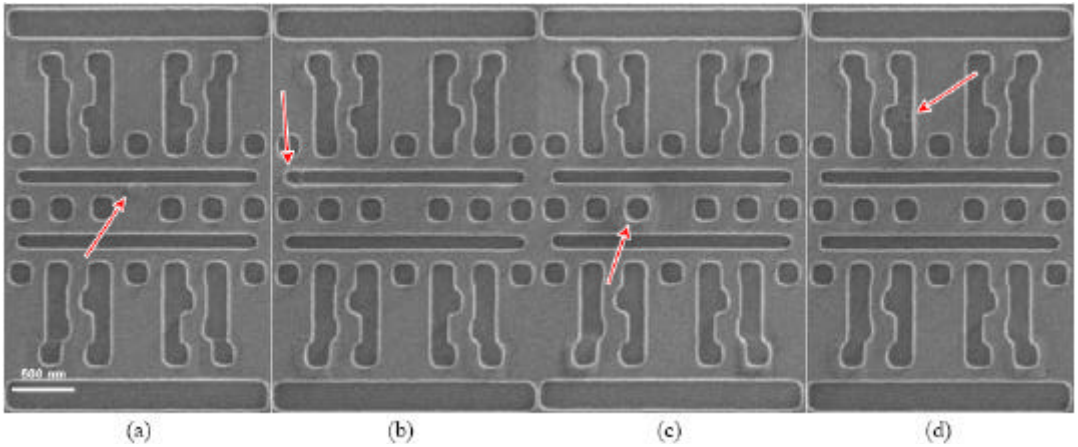

Figure 18. Repaired defects. An additive process is used in Figure 18a. Figures 18b-d depict subtractive repairs.

The corresponding imprints are shown in Figure 19. The imprint results show the exact replication of the repaired mask, with no observed imprinting anomalies. Again, note that the location of the defect is mirrored in x relative to the mask images, because of the imprint process. Figure 20 demonstrates the subtractive repair of the smallest programmed defects in this particular pattern.

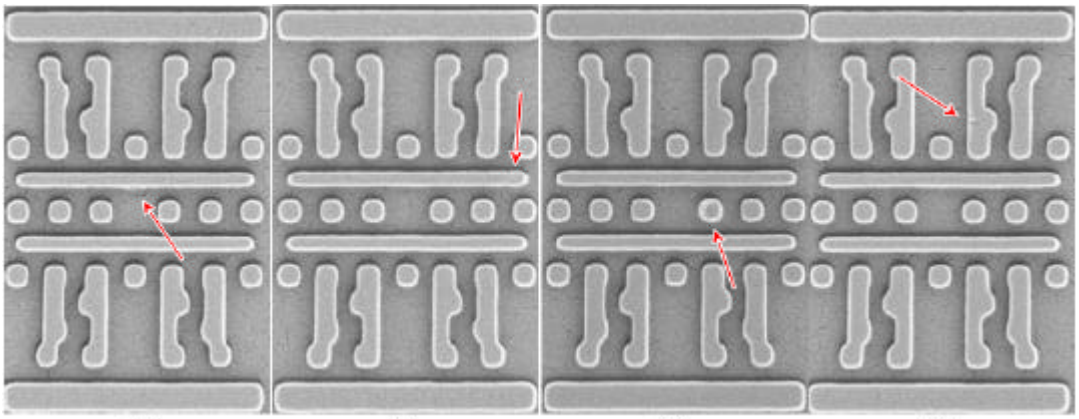

Figure 19. The corresponding imprints of the repaired patterns.

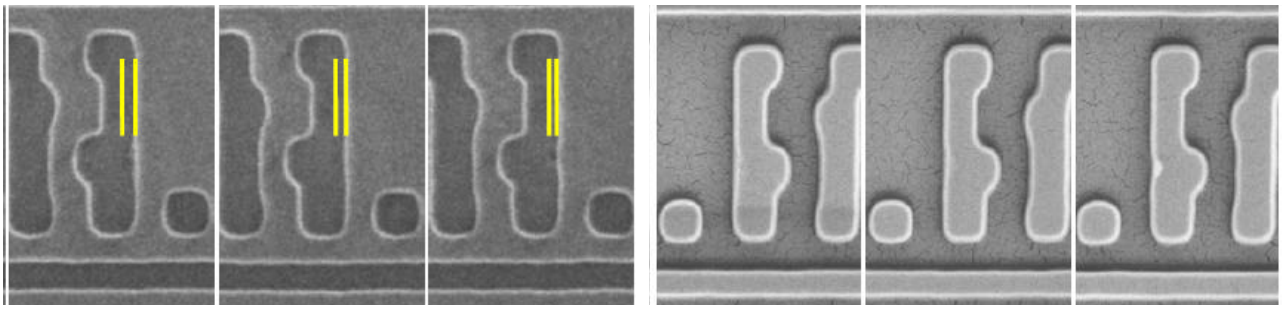

Figure 20. Left: Repaired features down to 32nm. Right: The corresponding imprinted patterns

As a final test, repair longevity was examined by imprinting 600 fields with the mask. Figure 21 shows the result of this experiment for both an additive mask repair (left) and a subtractive mask repair (right). No degradation was observed in either the mask or the imprinted wafers.

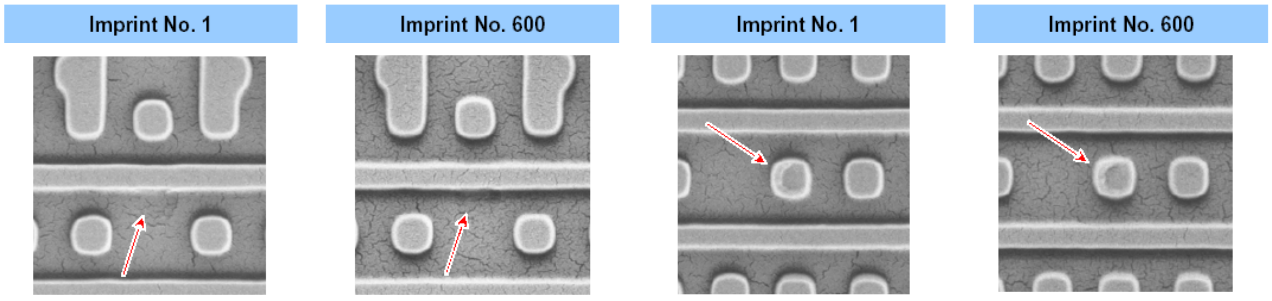

Figure 23. Left: an additive repair after imprint 1 and imprint 600. Right: a subtractive repair after imprint 1 and imprint 600.

4. Conclusion

The ITRS roadmap calls for sensitivity to 10 nm defects on an imprint mask for 22 nm NAND Flash design rules. The es35, at a pixel setting of 15 nm demonstrated the capability to detect defects as small as 10 nm, depending on defect type. The EScan 315 was able to detect several 8nm defects at a 10nm pixel setting. Inspection times still need to be reduced, however. As an example, for a 26 mm x 33 mm field inspection at 50 Mpps and a pixel size of 20 nm, approximately 12.5 hours would be required for the inspection. It is possible to increase data rates, but process development would be required to maintain the sensitivity levels demonstrated in this work. Finally, an eventual transition to direct inspection of the imprint mask, along with the ability to do die-to-database inspection would be beneficial. This work has also shown the feasibility for doing 1X mask repair down to 32nm. In the future, repairs will be attempted on the 32nm half pitch patterns used for inspection evaluation in this work.

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