In-line Semi-electrical Process Diagnosis Methodology for Integrated Process Window Optimization of 65nm and below Technology Nodes

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ABSTRACT

This paper presents the application of an innovative concept as potentially very powerful in-line diagnosis techniques in both process window optimization and yield enhancement for 65nm-and-below generations of technology. These applications were fulfilled with a novel methodology of the measurement and quantification of the grey levels on the SEM images and their correlation with the physical/electrical parameters of the semiconductor process steps. With these techniques & the few demonstrations, the virtual in-line semi-electrical measurement is proven to be a feasible technique in achieving technology development with lower cost and faster iteration cycle for continuous improvement. Else than technology development, the same techniques can also be served for the purposes of process window optimization and tool/ recipe/ process monitoring/qualification applications in volume production.

Keywords : voltage contrast, grey level, SEM, e-beam inspection, EBI methodology

1. INTRODUCTION

E-beam inspection (EBI) methodology has been widely used in integrated circuit industry for defining the very tiny or invisible but electrically fatal process faults with the superior image resolution and the well-known operation principle of ***Voltage Contrast*** (VC) [1-7]. The term of voltage contrast describes the observed visual contrast difference on the SEM image while a significant surface potential change occurred on the IC device. The drastically change of surface potential is often the result of the local charging redistribution on the surface of the IC device or structure caused by the IC process abnormality. The spatial resolution of the voltage contrast signal can be localized to precisely identify the spot that the process abnormality takes place thus this technique is widely used in in-line diagnosis or the off-line process failure analysis.

For in-line diagnosis applications, the amount and location of the VC signal is determined with the introduction of e-beam inspection tools instead of a traditional SEM. The e-beam inspection tool had demonstrated the effectiveness and the gained popularity while defect isolation became more and more challenging for the key process modules in sub-100nm technologies. However, with the e-beam exciting nature, the contrast level, or the grey level, observed on the inspection image could be further taken as the advantages to characterize the minor physical/electrical property differences of the IC structure or device.

In this work, the grey level values were extracted form the inspection images as the quantitative indices representing the structure or material properties such as the insulating film thickness above or in between the conductive materials. Then the correlation of the extracted grey level values with the physical properties was investigated and a calibration curve was established. With the calibrated relationship, the behavior of a set of test structures is easy to predict by in-line grey level measurement instead of traditional ways of electrical test confirmation or destructive cross-sectional analysis which are with longer cycle time and higher cost. According to the effectiveness of the method in quick determination of the process wellness, it was used for the guidance of process recipe tuning and the associated process

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window optimization. It is believed the technique will become a standard methodology in process development or production monitoring for 65nm-and-below technologies.

2. BASIC OPERATION PRINCIPLE

The grey level itself is the result of a series of the electronic signal amplification and analog-to-digital signal conversion process. Since the electronic signal source is the excited electrons form the material, the grey level values are different under different surface charging conditions even on the same test structure or device. The following paragraphs describe the basic operation principles of VC and grey level and give a simple model for interpretations of the grey level behavior under different surface charging conditions.

Operation Principle

When the primary electron beam of a SEM scans a portion of a device, secondary electrons (SE) and backscattered electrons (BSE) are excited. The number of SEs and BSEs excited per primary electron (PE) are called SE yield (δ) and BSE yield (η) respectively. A detector collects the emitted SE to form an image. The grey level of the image reveals the number of SE detected.

The total electron yield is defined as $\delta+\eta$. If the total electron yield does not equal to unity, positive or negative charges will be left behind on the scanned area. For a short circuit, these charges can be released instantly thus image grey level variation reveals the yield difference of materials as well as the topographical information. While for devices of high resistance, open or ground, charge accumulates on surface and builds up a local surface field (voltage) with which modulates the number of SE reaching the detector. The grey level variation closely correlates to the surface voltage difference, thus the image is called voltage contrast image.

Features with a positive voltage attract some SE back to the surface, the more positive the voltage reaches, the darker the image. Features with negative voltage reduce the landing energy of PE, which results in an increase of SE yield at the corresponding area, the more the negative voltage reaches, the higher the SE yield; then the features become brighter.

The level of voltage built up on the surface depends on the electrical characteristics of the device under scan. Once charging reached equilibrium, no further charge accumulates, thus current conservation law applies (see Fig,1).

$$\left.\frac{\partial Q}{\partial t}\right|_{t=\tau} = 0; \quad I_{PE}(1+\eta) + I_{SE}(\tau) + I_{SC}(\tau) = 0$$

Where $\boldsymbol{I_{PE}}$ refers to the primary beam current. It depends on system settings and remains unchanged while scanning; η is the BSE yield, $\boldsymbol{\eta\, I_{PE}} = \boldsymbol{I_{BSE}}$ is the BSE current excited by primary beam. Since BSE is of high energy, its yield is highly materials dependent. For a given material at given PE condition, the BSE current is independent of surface charging and can be regarded as a constant. τ is the time at which charging reached equilibrium. It is the RC time constant of the equivalent RC circuit of the structure. τ is usually much smaller than the pixel dwelling time (for instance 10ns), so equilibrium can be reached during a single scan. $\boldsymbol{I_{SE}(t)}$ refers to the SE current which is sensitive to different surface charging voltage; thus is time dependent. $\boldsymbol{I_{Sc}(t)}$ refers to the charging/discharge current via ground (substrate) or virtual ground. It is also time dependent and the direction is determined by the polarity of surface charging,

(1) If surface charged positive, $-\boldsymbol{I_{SE}(\tau)} = \boldsymbol{I_{PE}} + \boldsymbol{I_{BSE}} + |\, \boldsymbol{I_{Sc}(\tau)}\,|$, the higher the leak current, the higher the grey level becomes.
(2) If surface charged negative, $-\boldsymbol{I_{SE}(\tau)} = \boldsymbol{I_{PE}} + \boldsymbol{I_{BSE}} - |\, \boldsymbol{I_{Sc}(\tau)}\,|$, the higher the leak current, the lower the grey level becomes.
(3) If $\boldsymbol{I_{Sc}(\tau)} = 0$, i.e. no leak or short at all, regardless surface charge polarity, $-\boldsymbol{I_{SE}(\tau)} = \boldsymbol{I_{PE}} + \boldsymbol{I_{BSE}}$.

For the example given in Figure 1, we can employ a simplified RC model to illustrate the grey level of an SEM image of a device. Fig.1 (a) primary beam irradiates on a tungsten plug connecting to the N+/P-well, positive charges are induced and held on surface and bulk as the pn junction is reversed biased. At equilibrium, for ideal cases where no leak exists, $-I_{SE}(\tau) = I_{PE} + I_{BSE}$, which means the plug will show up in the same grey level as background dielectrics. If there are short or leakage between plug and P-well, electrons will follow from substrate to neutralize the positive charges. This enables PE to draw more SE current from the plug, i.e., $-I_{SE}(\tau) = I_{PE} + I_{BSE} + |I_{Sc}(\tau)|$, and makes the plug brighter than normal. The charging and discharge phenomenon of the device under the PE scanning can be simply analogy to a RC circuit as illustrated in (b). Short or leakage of the junction corresponds to the decrease of R or increase of C, thus the charging/discharging current is predominated by the R and C.

The similar model can be applied to other layers of semiconductor devices, such as contact, via, and etc. Since the grey level is directly correlated to the electrical property of a device being imaged, this methodology can be one of very powerful means to exam and diagnose various process characteristics on a wafer.

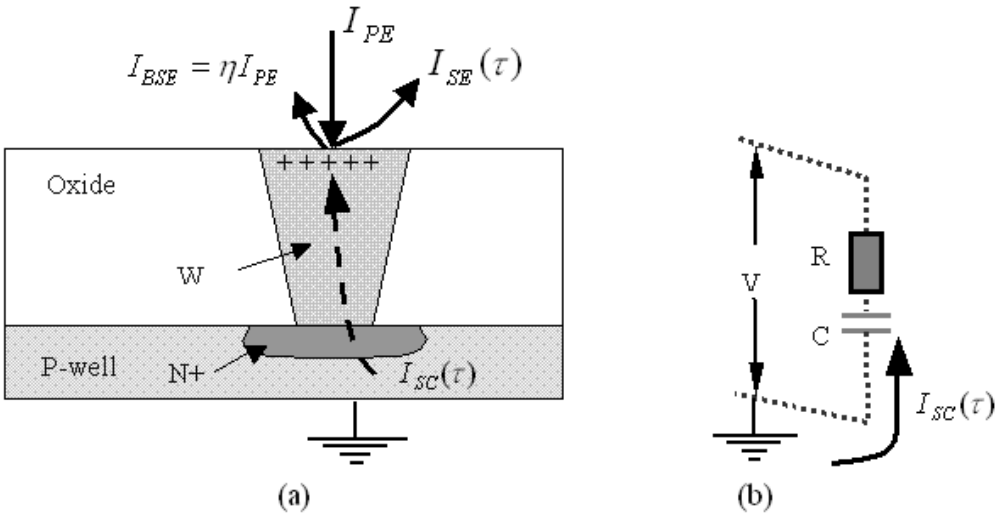

Figure 1. (a) The relationship of the incident primary beam current, the excited currents of the secondary electron and the back scattered electron and the substrate current in the case of positively surface charged W-plug connecting to a N+/PW junction (b) A simplified RC model

3. APPLICATION

The following application case will illustrate the utilization of the grey level method for semi-electrical process diagnosis and process window optimization.

3.1 Cu/Low-K BEOL via etching process window optimization

In this case, a robust Cu dual-damascene structure through optimization of via etching recipe is presented. For a Cu/Low-K dual damascene BEOL process, one of the most important factors to achieve high yield & reliable Cu dual-damascene process is to prevent the Etch Stop Layer (ESL) from being etched through during via/trench etch for a conventional via first integration scheme. The etched-through ESL may induce several fatal problems on Rc and reliability robustness of the Cu/Low-K interconnections so typically an amount of ESL film is remained atop the surface of the underneath Cu line after via etching till the removal of trench etching steps. Moreover, the remained ESL thickness among vias with different pitches from very dense to very isolated is required to be controlled within a certain range for the etching process to cover. However, for technology nodes of 65nm and below, the loading and micro-loading effects of the etching process are getting more predominant and much difficult to control. It is hard to use the traditional methods of cross sectional cut or other destructive techniques for the globally all-pitch ESL remaining check in an efficient way. The e-beam grey level method was thus employed for the purpose.

Correlation of e-beam grey level with ESL remaining

Fig.2 shows the e-beam grey level behaviors of via hole under various cases of ESL remaining after via etching process in which case the underneath Cu line is large enough to be served as virtual grounding. The measured grey level values track with the remained ESL thicknesses by TEM cross-sectional analysis. The observation can be easily interpreted with the similar model mentioned above. Fig.3 shows the schematic plot of etched via holes under e-beam excitation. In general a dielectric film surface tends to be negatively charged since the SE yield is <1 in the applicable range of landing energies. However for via hole, the very high aspect ratio nature further limits the amount of SE escaping from the via and collecting by the detector, so the pattern looks darker than the dielectric surface. The incident primary beam also charges negatively on the sidewall and bottom surface of via. At via bottom, the remained ESL film with the underneath Cu material behaves just like a capacitor accumulated with negative charges. In the case of sufficiently thick ESL remaining, the charging sustains and combines with the charging on the sidewall to form an electrical field to repel back the incident primary beam to the detector then the via hole looks brighter and thus the higher grey level value. But in the case of thinner or zero ESL remaining, the charges may not be well sustained but tunneled through the ESL down to the bottom plate (Cu). Since the combined electrical field is weaker, less electrons are repelled back so the via hole becomes darker and the corresponding grey level is lower.

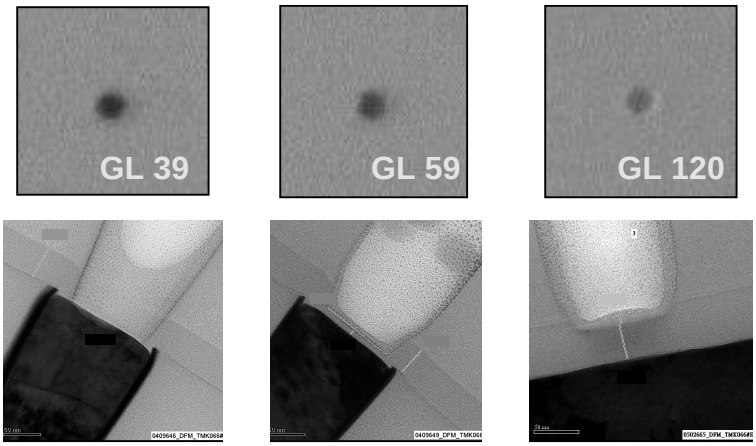

Figure 2. The measured e-beam grey level from a via-hole bottom under the cases of (a) ESL etching through (b) thin ESL remaining (c) thick ESL remaining.

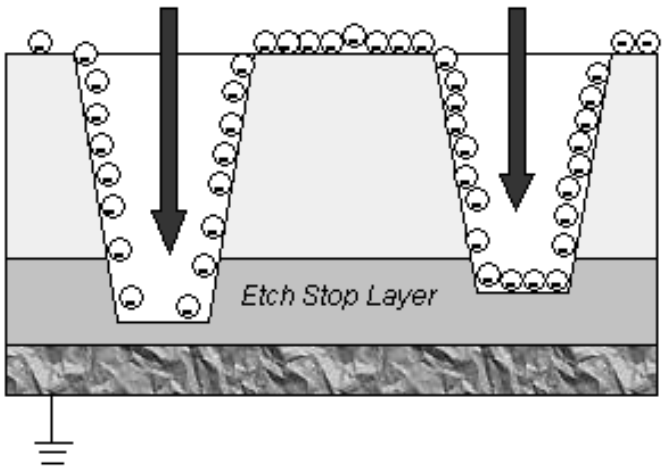

Fig.3 Schematic plot of etched via holes under e-beam excitation. The amount of negative charging built up on the IMD surface and via sidewall depends on the ESL remaining.

Based on the model, it is highly feasible to estimate the post-etch ESL remaining by measuring the e-beam grey level value as a direct index for process normality determination. This method was conducted non-destructively right after via etching steps where traditionally it is only doable after metal CMP either through convention VC or electrical probing. Fig.4 shows the calibration curve of the normalized remaining ESL thickness vs. the grey level. The solid triangle and the rectangle represent the two extreme cases of ESL etching through and underetch respectively. Traditionally VC method could well distinguish in qualitative way only for these two extreme cases but failed to tell more about the situations in-between. From the linear relationship between the ESL remaining and the grey level of sufficiently wide range, the curve can thus be adopted for the application of ESL remaining forecast and used to characterize an etch recipe or tool in-line.

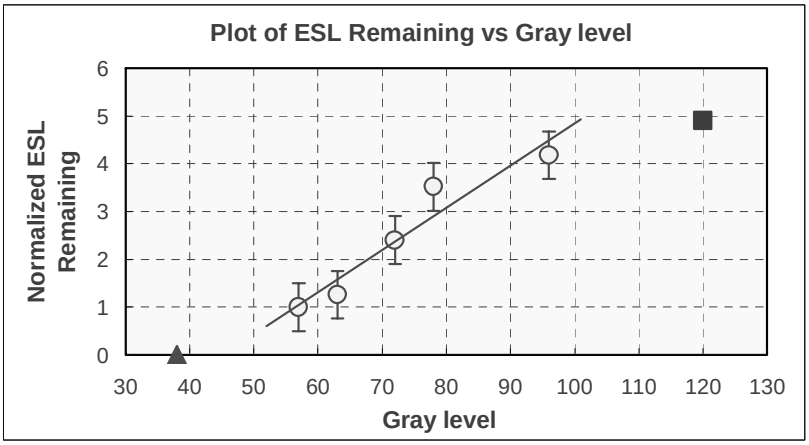

Fig.4 The good correlation of measured ebeam grey level value with the post-Via-etch physical ESL remaining

The grey level measurement is fulfilled automatically with an e-beam inspection tool at pre-programmed sites on a wafer. With the specially designed algorithm to automatically extracting the information from the SEM images, the quantified values provide a statistical database for further applications in via etching process window determination. For example, plots of wafer mapping can be generated from the database for across-wafer uniformity check (Fig.5). The grey level value from each measurement site stands for the local situation of ESL remaining. The local area with the risk to have either ESL etching through or underetch can be easily defined and the global picture of the process uniformity can be obtained instantly for process monitoring purpose.

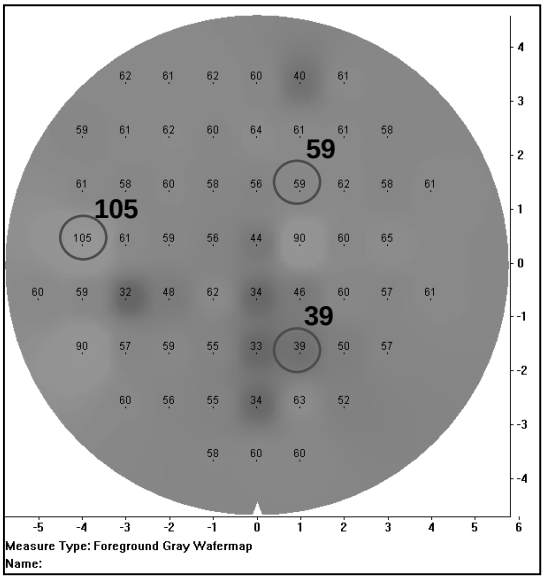

Fig.5 Example of grey level wafer mapping

Determination of common window through automatic grey level mapping

In addition to the instantaneous feedback of the in-line measurement, the methodology enables us to decouple the contributions from photo proximity and etching loading effects. The proximity effects for via patterning can be well characterized with existing methodology with accurate CD measurement however the characterization of the etching loading effect is still relied on cross-sectional cut to collect ESL remaining information (usually TEM). For process generations of 65nm and below with less within-wafer process variation tolerance, statistical information is required to describe the whole picture of the process uniformity. The TEM cut becomes nearly impossible to provide the required amount of information for the purpose.

Fig.6 shows the grey level mapping results on via patterns of dense, semi-dense and isolated pitches. The grey level data collection was through a single-pass measurement on the pre-programmed measurement sites with very short cycle time around 0.5hr. A database with statistical information is achieved by this non-destructive method. The observation of higher grey level for via with more isolate-pitch is consistent with the trend of loading effect. The mapping result also provides sufficient information with the spatial dependency for the process uniformity conclusion.

The collected database of grey level was further plotted as the cumulative probability plot (Fig.7). The common window of dense/sparse via is quickly determined through a preset box representing the tolerable range of grey level variation based on the calibration curve of ESL remaining vs. GL as described in Fig.4. The excursion point can be identified for further failure analysis to initiate next iteration of recipe tuning. With this methodology, via etching process optimization was able to achieve with faster but fewer iterations.

In addition to the usefulness on process monitoring and window optimization in technology development, the methodology is also useful in process tool recovery or matching for volume production. The grey level data collection is believed to be a very essential piece of information for the 65nm and below technology development and mass production in the means of quantitative manufacturability measurements.

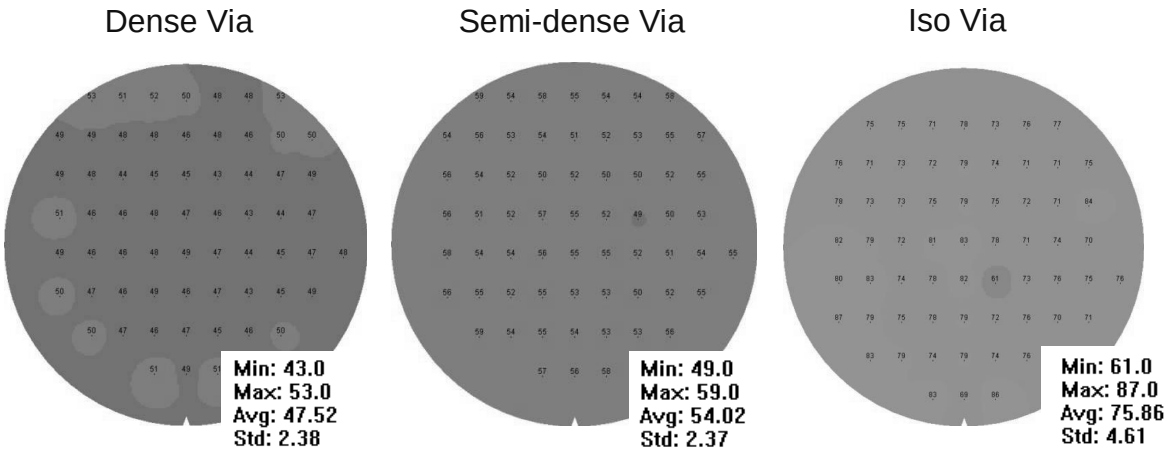

Fig.6 The grey level maps of (i) dense pitch (ii) semi-dense pitch and (iii) sparse via. The statistical information can be collected through a single-passed measurement with programmed measurement site.

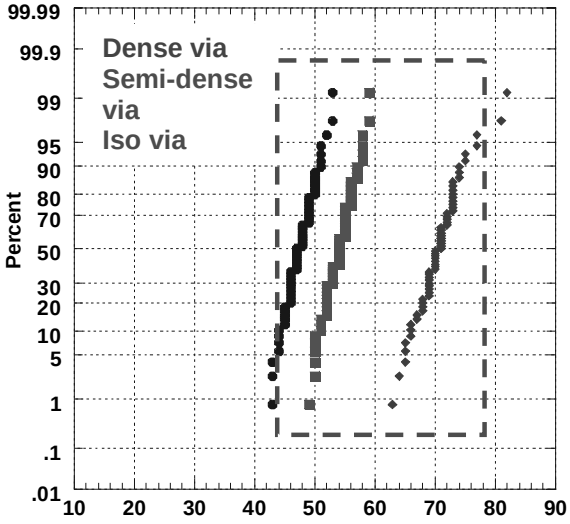

Fig.7 The quick determination of common process window of (i) dense pitch (ii) semi-dense pitch and (iii) sparse via by the non-destructive grey level mapping method

4. CONCLUSIONS

E-beam grey level measurement is an innovative technique and it is proven to be a very essential way to the advanced process technology development & manufacture window establishment. Its applications & usefulness are clearly demonstrated in the above example. The technique enables us to proceed to the level of in-line semi-electrical characterization for shortening the reaction cycle than traditional methods and to pinpoint the root cause without the cumbersome failure analysis in a statistical manner.

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