Implementation of Early Monitor by Advanced Ebeam Metrology for Charging Damage Failure Mechanism.

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Abstract

Based on failure analysis data the estimated failure mechanism in capacitor like device structures was simulated on wafer in Front End of Line. In the study the optimal process step for electron beam inspection (EBI) on Hermes Microvision eScanlite system was identified within various process steps. Finally an electron beam inspection monitor for early warning was established specifically to identify this fail mechanism with ADC (Automated Defect Classification) and statistical process control.

Keywords

FA, failure analysis, Voltage contrast, electrical fail mechanism, FEOL, front end of line, Hermes Microvision, HMI, eScanlite, e-beam inspection, EBI methodology, electrical defects, defect density, inspection, inspection system, inspection monitor, ADC, automatic defect classification, statistical process control, SPC, charging damage

INTRODUCTION

Electron beam has been increasingly used for defect inspection in IC chip fabrication because of the shrinking of the killer defects' dimensions beyond the capability of optical defect inspection equipment. In addition to detecting the tiny physical defects due to its high resolution, the unique capability of an e-beam is detecting electrical defects such as shorts or leaky circuits and open or partially open circuits, which makes it an equipment of choice for front-end of line (FEOL) and interconnect process inspections and monitoring. eScan®Lite is an e-beam inspection system developed by HMI.

Its e-beam system consists of an electron gun, an e-beam column, objective apertures, an annular semiconductor detector to detect both secondary electrons (SE) and back scattered electrons (BSE). Please refer to Figure 1.

When the electrons in the focused primary beam hit the tiny spot (a pixel from 30 to 100 nm) on the wafer surface, they will excite many SE and BSE, as well as some other electrons and photons out of the material surface it interacts with. The brightness or the gray level value (GLV) of the pixel in an SEM image is determined by the

total number of electrons from this pixel that reach the detector.

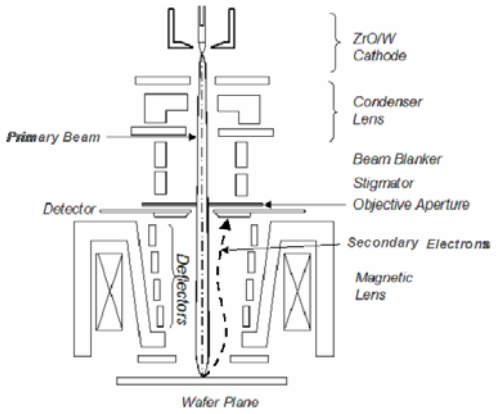

Figure 1. Schematics of electron-beam system of eScanLite

An SEM image is formed at the same sampled locations of different dies. By comparing the GLV difference of the pixels of the images in different dies, defects can be detected on a product wafer using non-destructive, in-line process monitoring. The landing energy (LE) of 250 to 2500eV of the primary electron beam can be controlled by the total bias between electron gun and wafer. The relationship of LE and yield rate of the SE, BSE and their combinations are shown in Figure 2. It shows that when E1<LE<E2, more electrons leave the surface than reach it, thus inducing positive charge on the surface. Inspections described in this paper are performed in this regime, which is called "positive mode".

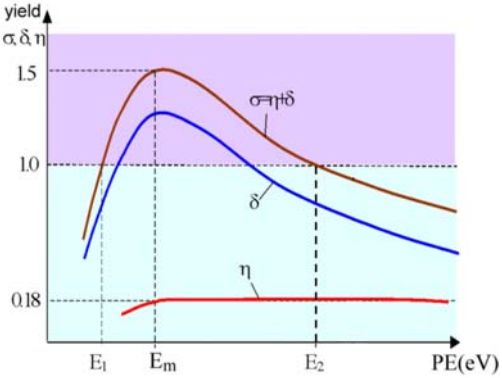

Figure 2. Relationship of landing energy of primary beam with SE/ BSE yields

To identify electrical fail mechanism in early stage of wafer flow, several e-Beam inspection steps are established within the line of Infineon Dresden.
In this particular case the use of e-beam inspection was driven by failure analysis results, pointing out electrical fail mechanism in early front end of line (FEOL). Photo Emission Microscopy spots were located in a capacitor device. Electrical analysis indicated gate oxide breakthrough. Finally the chips fails could be correlated to an etch process on one specific chamber.
The main limiting factor for a root cause analysis and experiments to narrow down the kind of fail mechanism was the long feedback time from the critical process step in early front end of line to the electrical test – refer to Figure3. For lots it takes several weeks to reach the electrical test. Accelerated lots can narrow down the time towards two weeks at high logistics cost.
The ideal solution would be an inline e-Beam inspection close to the faulty etch process.

EXPERIMENTAL SETUP

The electrical fail mechanism was already characterized as a leakage issue in a capacitor device structure. It appeared in fail signatures across the wafer. The open question was, if e-beam would be capable to detect the fail mechanism inline.

An answer could be provided with the method of electrical device simulation including all electrical parameters inside the modeling (e.g. SPICE simulation). However simulation models results have often gaps to real technology. The models provide mostly a rough estimation on the order of magnitude.

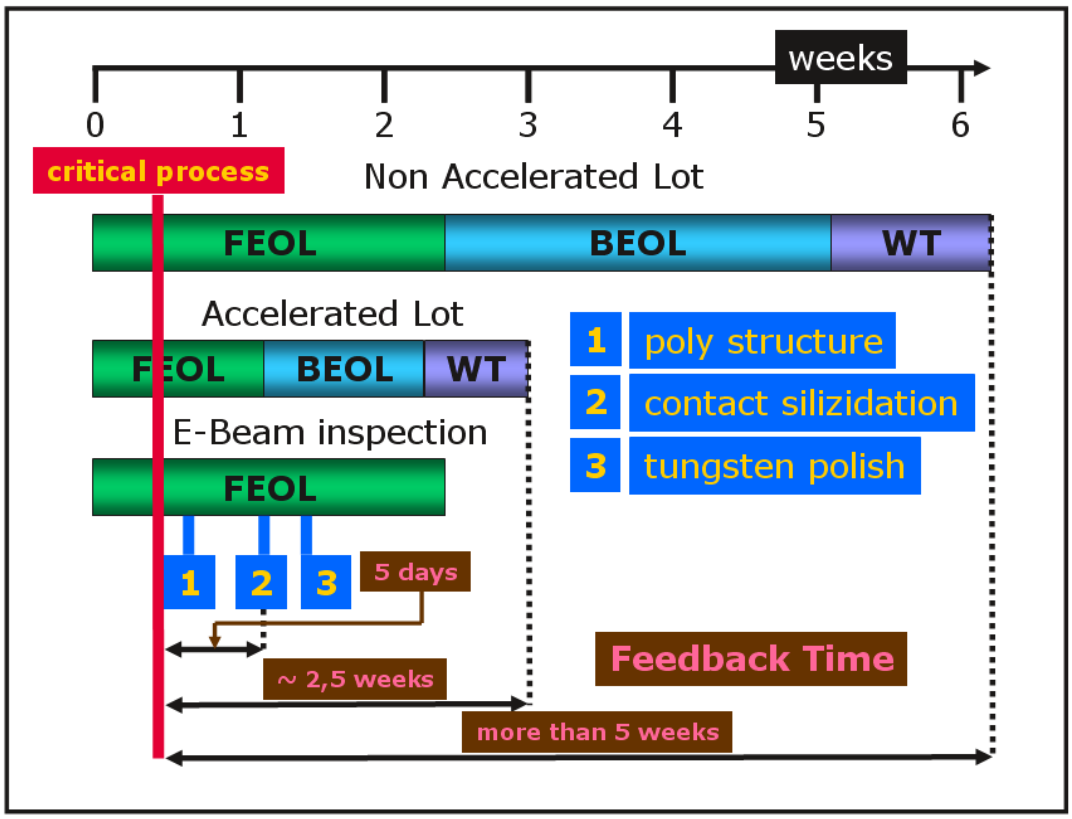

Figure 3. Time delay in the feedback loops to monitor the critical process for (non) accelerated lots as well as for e-beam inspection.

The other way and from the author at Infineon well established real successful method is to create artificially defects that simulate the electrical fail mechanism. In this particular case capacitors were specifically prepared with leaks in the gate oxide by use of inline focus ion beam.

One wafer was prepared on two dies with the artificial leakage defects in gate oxide. See figure4.

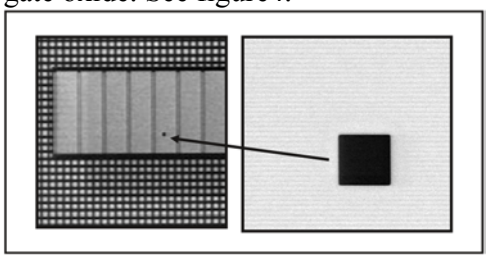

Figure 4. Example image of artificial gate oxide leakage defect in the capacitor device.

The next step was to select the best possible process for voltage contrast e-beam inspection on this capacitors (see figure5):

1. Post poly silicon deposition & structuring & doping
2. Post gate and contact silicidation
3. Post tungsten chemical mechanical polish

RESULTS

The wafer with the artificial leaks in the capacitor was inspected at each of the three selected process steps. At each process step the known leaking locations were selected by their coordinates and e-beam voltage contrast settings were selected that provide a maximal signal to noise ratio for the capacitor leaks. At the end at each of the steps the e-beam recipe had very good signal to noise ratio for capture of the artificial leaks with good capture rate. Refer to figure6.

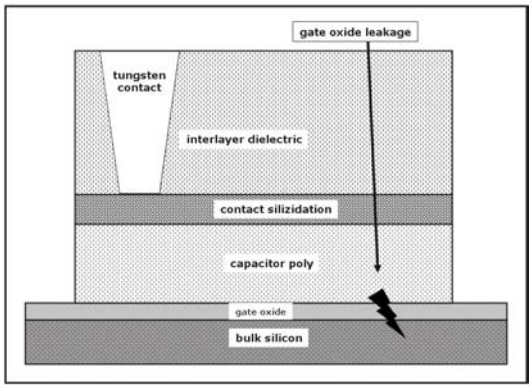

Figure 5. Simplified process stack until tungsten chemical mechanical polish for the capacitor device. The leakage in gate oxide is indicated.

To prove that the artificial leak simulated well the real electrical fault, several product wafer were processed over the critical etch chamber under worst case condition.

from the nuisance defects across the whole wafer map.
Post contact silizidation the defects appeared clearly among other really or nuisance type defects. Finally the leaking capacitors could be precisely separated by use of automatic defect classification (ADC) for this step.

Post tungsten chemical mechanical polish the leaking capacitors could be detected but with just weak signal to noise ratio for detection and the general nuisance level was high.

At the end the contact silizidation step was selected for an inline monitoring. Automatic trend charts were established on the defect type of leaking capacitor structures and violation limits were set.

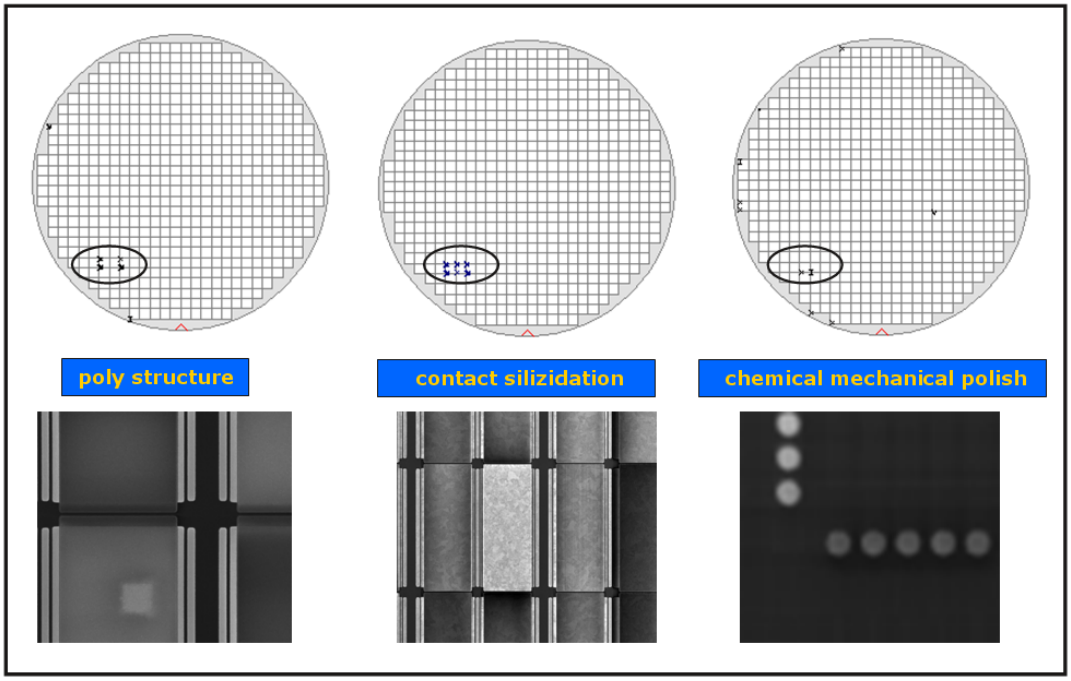

Figure 6. Defect maps of different e-beam inspection steps and defect examples images.

The product wafers were inspected with the e-beam at each of the tree above mentioned process steps.
At the post poly structuring step the defects could not be differentiated

CONCLUSION

Due to the excellent detection of the leaking capacitors after gate silizidation by e-beam inspection, the results of experiments and further intense root cause analysis for the etch chamber

was available just some days later. Refer to figure7.

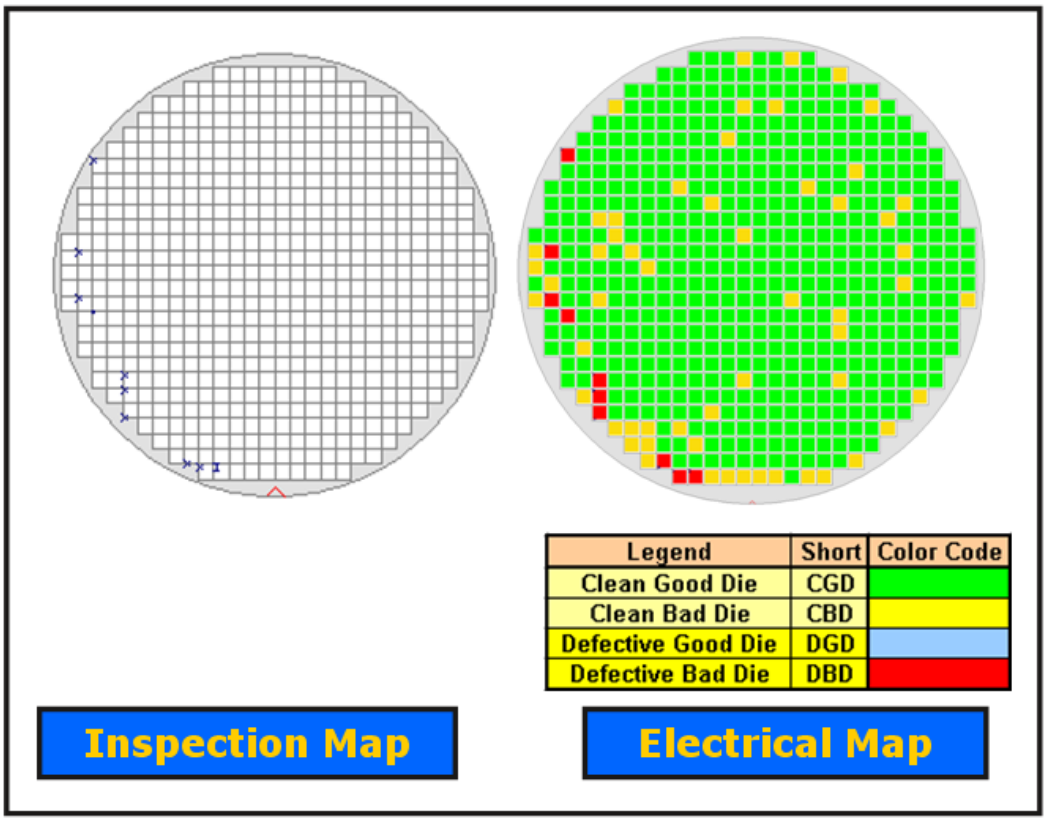

Figure 7. Correlation between automatic defect classified map in contact silizidation and the electrical test map.

Due to the fast results new iteration of experiments could be done.
The iteration speed of the feedback loop was shortening from approximately six weeks to about 5 days.
It proves that the method of forced electrical failures is very helpful for the selection of the right inspection step within the workflow and optimization of e-beam parameters. In some cases it turned out to be the only key for successful e-beam use.