Enhancing Thin Dielectric Remaining Detection Under Polysilico Plug of Advanced DRAM by Electron Beam Inspection

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Abstract

We've studied using negative mode e-beam inspection (EBI) to detect a thin layer of dielectric remain at the bottom of storage node contact (SNC) hole. A thin layer (~15 nm) of nitride at the bottom of some SNC holes was intentionally created, EBI were performed at two stages: post etch clean and after silicon nitride cap of SNC plug. Negative mode EBI after SNC nitride cap deposition successfully captured these contact open defects as bright voltage contrast (BVC) defects. The cross-section scanning electron microscope (SEM) confirmed the results. The inspection mechanism is also discussed in the paper. We found that negative mode EBI is very useful for in-line defect monitoring.

Introduction

EBI systems are widely used for monitoring contact processes. [1], [2] It has also been used for contact process window qualification. [3] Figure 1 illustrates the DRAM contacts, such as self-aligned contact (SAC), bit line contact (BLC) and SNC. Two defects of interest (DOI) are illustrated in Figure 1, SAC open and SNC open. When critical dimension (CD) shrinks, contact etch processes become more challenging, and monitoring the yield limiting dielectric remain due to under etch becomes more and more important. Normally, the contact processes are monitored with EBI in after etch inspection (AEI) or after polysilicon chemical mechanical polish (CMP). However, for SNC process, it is difficult to detect a very thin layer of dielectric remain (~15nm) at bottom of the SNC holes, especially when the SAC polysilicon they landed on has not been annealed. Even after polysilicon CMP, the defect detection rate is still very low. Therefore, a novel EBI mechanism is needed to catch this DOI.

Negative EBI with Nitride Cap

The relationship between electron beam landing energy (LE) and yield rates of secondary electron (SE) and back scattered electron (BSE) are shown in Figure 2. [4] When $LE>E_2$, sample surface tends to charge negatively and EBI in this regime is called negative mode. Voltage contrast (VC) behavior of polysilicon plug underneath the nitride cap layer in negative mode EBI is illustrated in Figure 3. For plugs that contact to ground, local electric field will be formed between plugs and cap surface, which prevents SE from leaving the surface and reaching the detector. Therefore, the gray level (GL) of the nitride on top and around the ground plugs is low. In DRAM cell area, all plugs are connected to N+/P-well, which are forward biased in negative mode, thus equivalent to connect to ground. A thin layer of dielectric remain underneath a plug can block the path of electrons to the substrate and makes the plug become floated. This minimizes the local electric field between the plug and the cap layer surface, and more SE on top and around the plug can leave surface and reach detector. Therefore, dielectric remain induced contact open can be captured as BVC defect.

Experiment Results

To test the theory, a DRAM wafer with known contact open issue at SAC layer was inspected using HMI's eScan®300 after SNC nitride cap deposition. Figure 4a is the multiple BVC defect map and Figure 4b is a review image of the multiple BVC. Figure 5a shows the single BVC defect map and Figure 5b shows the single BVC defect review image. This experiment proved that negative mode inspection at nitride cap of polysilicon plugs can capture contact open defects.

To simulate under etch induced thin dielectric remain at the bottom SNC, we intentionally applied polystyrene latex (PSL) spheres on a certain area of a DRAM wafer after SNC nitride liner (~15nm) deposition. A plasma etchback process removes the nitride film from the wafer surface and the bottom of SNC holes while leaving nitride film on the sidewall of holes to prevent electrical short between SNC polysilicon plugs and the bit lines. For the holes that blocked by PSL spheres, nitride film at the bottom of holes most likely will be left behind, which can cause open circuit of the plugs. Figure 6 illustrates the process and inspection sequence.

Dark field optical inspection after nitride etchback (Step A) captured PSL spheres in the care area and it was confirmed by review SEM. Figure 7a shows the defect map and Figure 7b is the detail defect distribution in the area that PSL spheres were applied. Figure 8a and Figure 8b are the review SEM images of PSL spheres. PSL spheres were removed by a wet clean process (Step B). EBI after Step B did not capture any contact open defect, due to the lower sensitivity at that layer to the thin nitride remain. The wafer then went through polysilicon deposition and polysilicon

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CMP. After nitride cap deposition (Step C), negative mode EBI was performed. It has much higher sensitivity to the thin dielectric remain. It captured the DOI, PSL sphere induced SNC opens, as BVC defects, shown in Figure 9a and Figure 9b. Figure 10a is the BVC defect map and Figure 10b is the detail defect distribution in the care area. For total 44 BVC defects captured with EBI, 25 of them are located at the same sites in dark field inspection map, marked with circles in both Figure 7b and Figure 10b. Figure 11 is the defect counts summary of the three inspections. Cross-section SEM image in Figure 12 confirmed that the BVC defect was caused by the thin nitride remain.

Discussion

EBI of one of DOI, contact open with very thin dielectric remain on the bottom of holes, were performed on a DRAM wafer at two steps: SNC nitride liner etchback and SNC nitride cap deposition. We found that the sensitivity to capture this DOI is much higher at SNC nitride cap with negative mode inspection. For EBI at nitride cap, the local electric field in nitride layer directly affects the number of SE from surface to reach detector. For EBI at contact etch, majority of SE from the hole bottom were hit the sidewall of the hole, only small portion of them can reach detector, thus signal to noise ratio is low and sensitivity to bottom remain is low. Other contributing factor is after nitride cap deposition, the polysilicon plug in both SNC and SAC were annealed by the thermal process, which provide a lower resistance path to the ground. When inspection was at the SNC etch, the SAC polysilicon plugs hadn't been annealed, therefore had high resistance to the ground and low sensitivity to thin dielectric reamin..

Summary

In this study we've found that negative mode EBI after nitride cap is very effective to capture polysilicon plug open circuit to the substrate caused by thin dielectric remain due to under etch. It can be used for monitoring SNC and SAC processes.

Acknowledgement

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References

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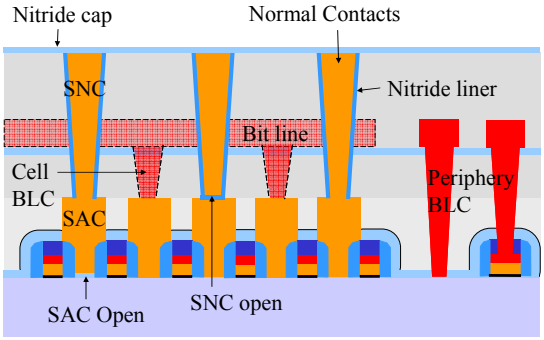


Figure 1. Illustration of DRAM contacts, SAC, BLC and SNC. Bit line and BLC in cell area with dash line to indicate there are behind the cross-section.

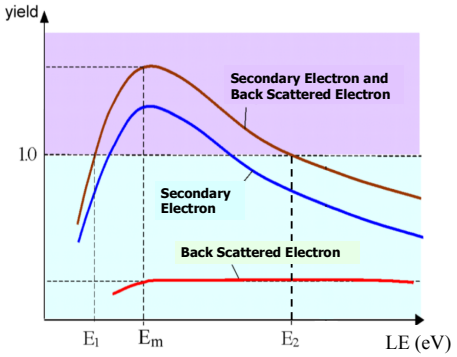


Figure 2. LE of e-beam and SE and BSE yields.

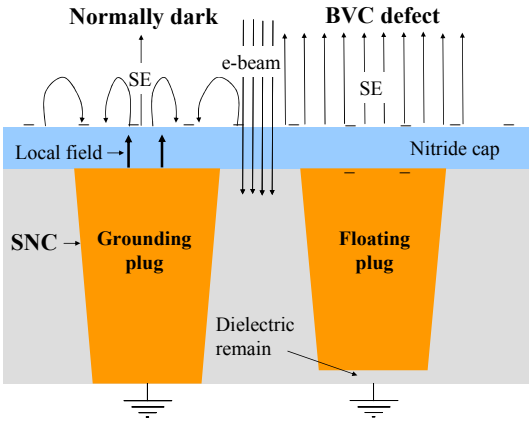
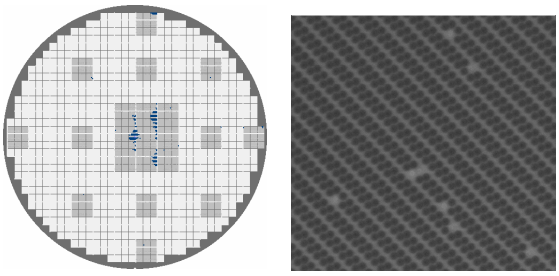
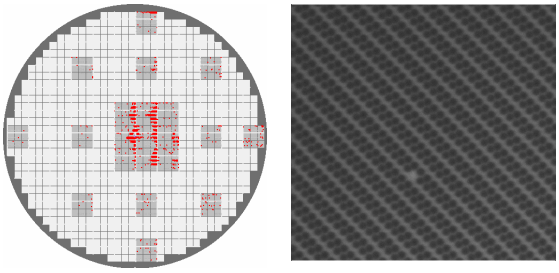


Figure 3. Negative mode VC behavior of polysilicon plugs with nitride cap.



(a) (b)

Figure 4. (a) Multi BVC defect map. (b) eScan®300 review image of multiple BVC defect.

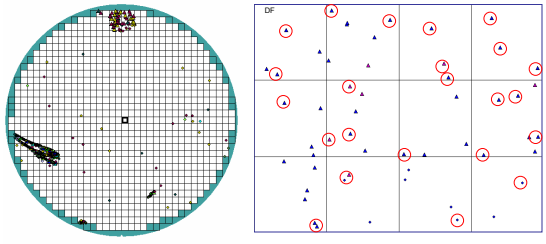


(a) (b)

Figure 5. (a) Single BVC defect map. (b) eScan®300 review image of single BVC defect.

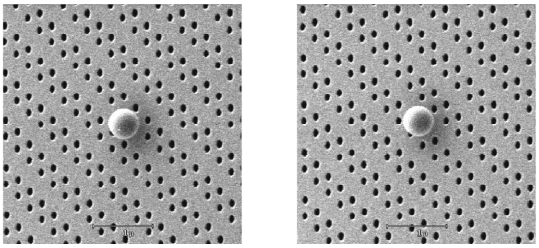
- SNC etch
- Clean
- Nitride liner deposition
- PSL spheres
- Nitride etch back
- **DF inspection**
- Clean
- **1st EBI**
- Poly deposition
- Poly CMP
- Nitride cap
- **2nd EBI**

Figure 6. Process and inspection sequence.



(a) (b)

Figure 7. (a) Dark field inspection defect map. (b) Detail defect distribution in area where the PSL spheres are applied.



(a) (b)

Figure 8. (a) and (b) Review SEM images of PSL spheres.

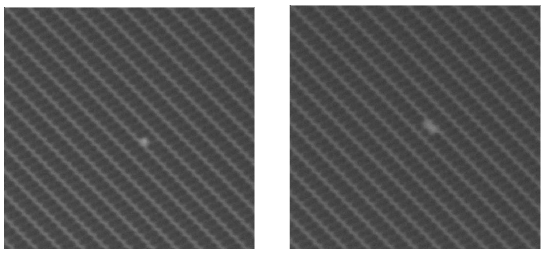
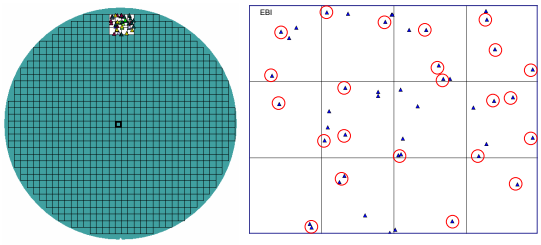


Figure 9. (a) and (b) eScan®300 review images of BVC defects.



(a) (b)

Figure 10. (a) EBI defect map. (b) Detail defect distribution in area where the PSL spheres are applied.

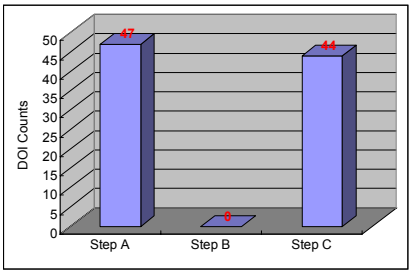


Figure 11. Dark field optical inspection DOI (PSL spheres) count after Step A and EBI DOI (BVC) count after Step B and step C.

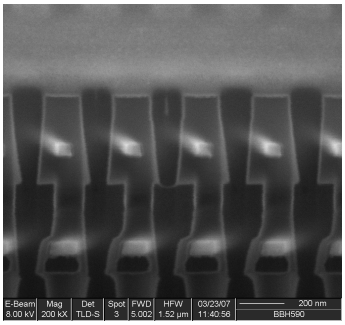


Figure 12. Cross-section SEM showed the thin nitride remain at bottom of SNC that caused single BVC in SNC cap negative mode EBI

Author Biography

Luke Lin, PhD, is a department manager of yield engineering department at Powerchip Semiconductor Company (PSC) Fab 12A/B in Hsin-Chu, Taiwan. He has over 10 years of experience in the areas of surface analysis, 200 mm / 300 mm defect metrology and particles/yield improvement in 300 mm DRAM production line. He has Ph.D. degree in Physical Chemistry from the National Tsing-Hua University, and B.A. degree from Tamkang University in Taiwan. Prior to joining PSC, he worked in the area of semiconductor CVD process at Taisil Electronic Material Company in Taiwan.