Enhancement of Voltage Contrast Inspection Signal Using Scan Direction

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Abstract – **In-line voltage contrast inspection has taken off in popularity in the last decade. While the impact of this technique has already been dramatic, the best known practices are still rapidly evolving. This paper shows that scan direction can have a very large influence on signal intensity for defects of interest and that flexibility to be able to scan in both the X and Y directions can prove very advantageous. Two examples are presented illustrating this point. The underlying physics behind this phenomenon are explained. A new best practice for voltage contrast inspection is then proposed.**

INTRODUCTION

Effective use of in-line voltage contrast (VC) inspection can substantially accelerate yield ramp. This is because critical defects, otherwise only detectable weeks or months after their formation, can be detected within days. In-line VC inspection therefore provides a metric for fast turn-around of integration split experiments. It can also be used to monitor for process excursions which can degrade the yield for an entire wave of hardware.

In-line VC inspection is still relatively new; the first electron beam inspection tool was offered on the general market around 1996. Because of this, the best practices for using this technology are rapidly evolving [1-8]. At the same time, the theory explaining the phenomena observed during practical application of e-beam inspection is also maturing [9-11].

One of the key challenges is to improve the sensitivity of VC inspection to more subtle VC defects. Defects may be more difficult to detect for two reasons:

- The difference in grounding between a defective structure and a good structure is small.
- The defect is resistive rather than a hard open or short.

Development of techniques to improve the sensitive and the speed of recipe development in these scenarios is needed.

This paper shows that scan direction can have a very large influence on signal intensity for defects of interest (DOIs) and that the flexibility to be able to scan in both the X and Y direction can prove very advantageous. Two examples are presented in Sections 2 and 3 illustrating this point. The physics explaining this phenomenon are explained within these sections Section 4 describes a best practice to address this phenomenon.

CASE 1: SRAMs WITH SMALL N WELL REGIONS

Figure 1 shows two different SRAM cells for a recent bulk technology. The layout of these cells is quite typical throughout the industry. SRAM 1 has a strong VC signal whereas the signal for SRAM 2 is quite weak. A strong VC signal means the difference in brightness between the PFET contacts (CAs) and NFET CAs is quite substantial. These images are from WCMP, the most common inspection point, but the signal at other inspection points, specifically silicide anneal and metal 1, is similar.

For SRAM 1, the CAs landing on NFETs are dark whereas the contacts landing on the PFETs are bright. This is because, under the positive mode (aka electron extracting) conditions used for these images, the PFET active regions are forward biased to the N well which acts as a large virtual ground. PFET CA opens are therefore very easy to detect because of the large difference in grounding between good and bad CAs. The NFET active regions on the other hand are isolated from the P region underneath and therefore the intensity difference between good and bad CAs is very small. Typically, PFET CAs are inspected for opens while NFET CAs are inspected for shorts. Note that NFET CAs can also be detected if the threshold is set very low and a number of nuisance defects is acceptable.

One would expect a similar signal, where the PFET CAs are much brighter than the NFET CAs, for SRAM 2, but this is not the case. Comparison of the SRAM designs shows that the N well regions of SRAM 1 are tied together at the bottom and top of each SRAM block. This is not so for SRAM 2. See Figs. 2 and 3. The result is that the N well for SRAM 1 is more than 100 times larger than for SRAM 2. Therefore it provides much more virtual grounding for the PFET CAs. Table 1 shows the size of the N well for

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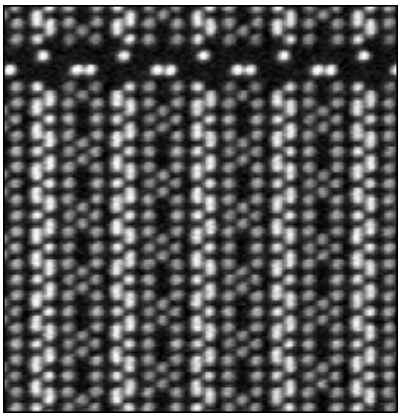
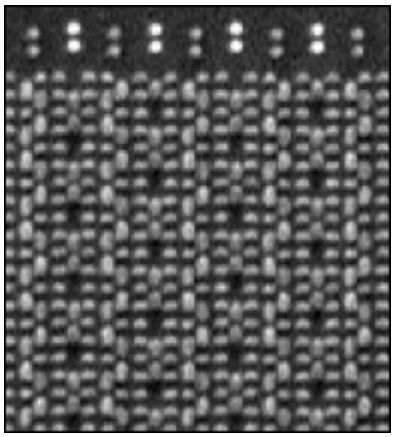
each of these SRAMs as well as a sampling of others. This data shows the intensity difference is related to the size of the N well. Sizes greater than 100 um2 provided sufficient grounding for this technology.



SRAM 1



SRAM 2

Figure 1: The appearance of two different SRAMs at WCMP under electron extracting conditions. The PFET CAs are much brighter than the NFET CAs for SRAM 1. This is not the case for SRAM 2.

Based on the image in Fig. 1, it does not appear that SRAM 2 can be effectively inspected. By switching to a Y direction scan, however, a much better signal was obtained. See Fig. 4. (Note that X direction is the intuitive direction for scan because SRAMs blocks are wide but not very tall. An X direction scan minimizes the number of swathes.) To understand why, the operation of an inspection SEM must be reviewed.

In order to rapidly scan large areas with high resolution, the wafer is loaded on a stage and moved in one direction while the electron beam and collection optics are rastered in the second direction as shown in Fig. 5. If the stage is moved in the X direction as was done for Fig. 1, the raster is in the Y direction. The N wells in SRAM 2 are scanned sequentially so that each N well is scanned in a very short time. On the other hand, if the stage is moved in the Y direction as for Fig. 4, then the raster is in the X direction. All the N wells in a swath width are scanned together over a much longer period of time. Since the charge has much more time to leak away, much less change builds up in the N well, and the PFET CAs appear much brighter than the NFET CAs.

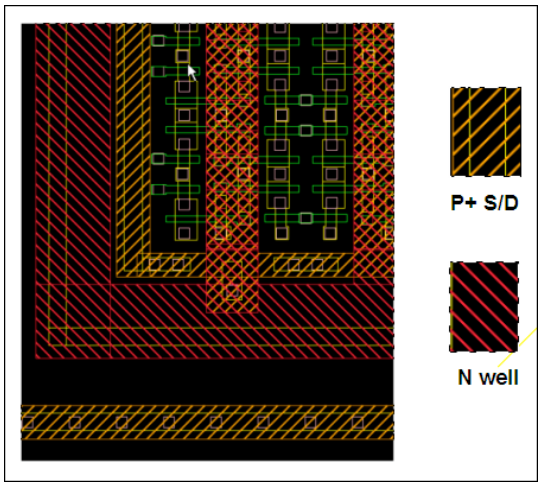


Figure 2: The layout for SRAM 1. Each N well is shared for all the PFET contacts in each column and the columns are tied together.

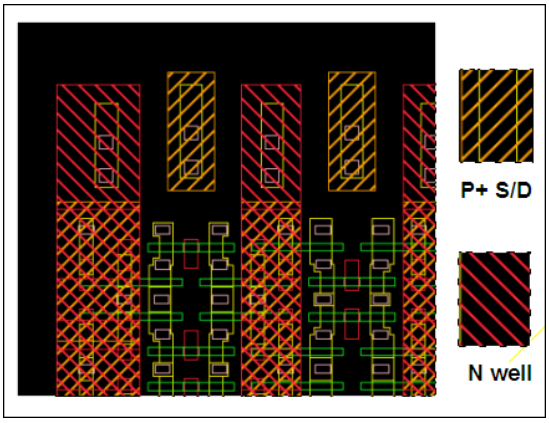


Figure 3: The layout for SRAM 2. The N well is shared by the PFET contacts in each column, but the columns are not tied together.

Based on these findings, SRAM layouts have been modified at IBM to maximize the N well area and therefore the VC signal. These changes allow flexibility in VC inspection set up. Even though good sensitivity to opens and shorts can be obtained by scanning in the Y direction, scan in the X direction is still preferable. First, fewer swaths are needed resulting in a faster inspection. Second, because of wafer to wafer alignment accuracy, a several microns at the edge of each care area block must be excluded to ensure the edge of the block is not caught. For a short care area as when scanning in the Y direction a very large amount of the SRAM area is lost.

Table 1: VC signal versus N well size

	total (um^2)	VC signal
SRAM 3	13	bad
SRAM 2	19	bad
SRAM 4	134	good
SRAM 5	507	good
SRAM 6	1232	good
SRAM 1	3390	good

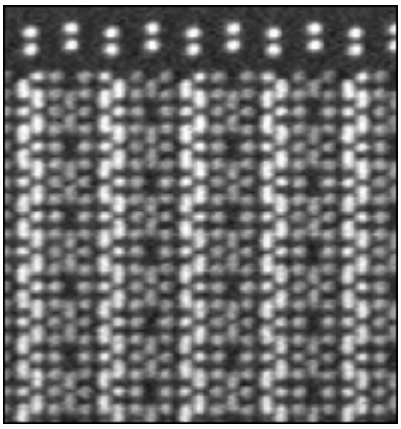


Figure 4: SRAM 2 when scanned in the Y direction. There is now a strong voltage contrast difference between PFET contacts and NFET contacts. The inspection is again at WCMP and under electron extracting conditions.

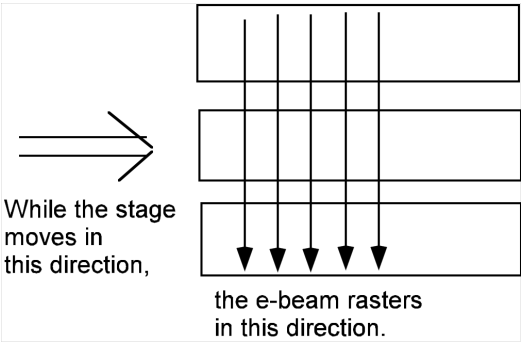


Figure 5: E-beam inspection tool scan dynamics. In this diagram, the wafer is moved in the X direction while the electron beam and collection optics are rastered in the Y direction. The rectangles represent SRAM blocks. This was how the images in Fig. 1 were collected. The image in Fig. 4 was collected with the stage moving in downwards and the e-beam rastering left to right.

CASE 2: WORD-LINE TO WORD-LINE SHORTS

The second example shows that word-line (WL) to word-line CA shorts within a bulk SRAM cell can be easily picked up with a scan in the Y direction but not with an X direction scan. Figure 6 shows an example high resolution image of this defect type. The word-line contacts, which for this SRAM cell are rectangular, may in some situations short. When scanned in the Y direction, these defects generate the VC signal shown in Fig. 7. An X direction scan does not show this signal. The reason is similar to the reason for the first example. When scanned in the Y direction with the electron beam rastering left and right, the pair of merged word-line contacts is scanned over a much longer time period allowing it more time to discharge.

These examples suggest that careful consideration of the scan direction to maximize voltage contrast signal intensity is a best practice. Fujiyoshi et. al. reports a similar finding but in the context of failure analysis [12]. Furthermore, actually trying scans in both directions during the setup of new inspections would be very useful in many cases.

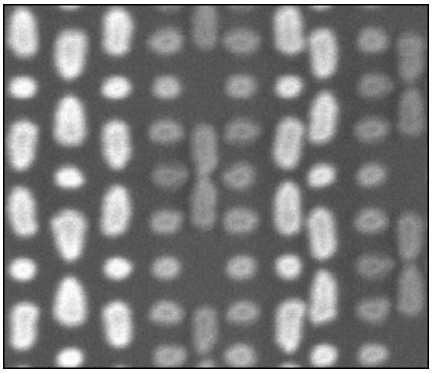


Figure 6: High resolution image of WL to WL short.

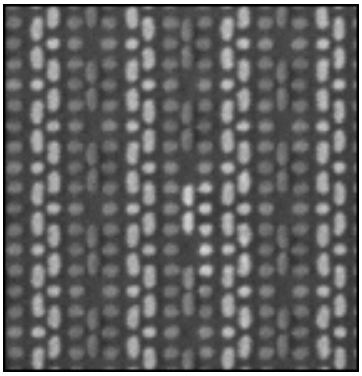


Figure 7: Voltage contrast signal for a WL to WL short when scanned in the Y direction. Notice the shorted pair of word-lines is brighter than the other word-lines.

PRACTICAL APPLICATION

Often the advantages to be gained by scanning in the alternate direction are not clear until tried. The e-beam inspection tool used for this work, the HMI eScan 380, unlike other commercially available tools, is able to scan in both the X and Y directions regardless of the way the wafer is aligned. This allows both scan directions to be explored very quickly with a single recipe. With tools that can only scan in one direction, two separate recipe setups are required and the wafer must be unloaded to switch between them.

Furthermore, with this inspection SEM, it is possible to create an inspection where some care areas are scanned in the X direction and others are scanned in the Y direction. This proves advantageous in situations where multiple care areas are needed where some are most effectively scanned in the X direction while others are most effectively scanned in the Y direction. In some situations it may make sense to scan a particular SRAM in both directions to capture different DOIs. The eScan 380 provides the flexibility to pursue these options within a single inspection.

CONCLUSIONS

This paper shows that scan direction can have a very large influence on signal intensity for defects of interest. Two examples were used to illustrate this point. The first example showed that scanning SRAM in the Y direction results in a much stronger VC signal for SRAM with small N wells. The second example shows that scanning SRAM in the Y direction makes detection of word-line to word-line shorts possible. This improved sensitivity is due to the substantially lengthen time used to scan the electrical nodes of interest. Based on these observations, we recommend as a best practice, trying both scan directions for many initial inspection setups.

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