

Effects of WCMP Process on Surface Charging Mode of Electron Beam Inspection

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Abstract

In this study, we've found that tungsten chemical mechanical polish (WCMP) process can strongly affect surface charging modes of electron beam inspection (EBI). We have changed WCMP process by using different slurry to modified surface condition to solve the mix charging mode issue and achieved negative mode electron beam inspection (EBI). We detected dark voltage contrast (DVC) defects on PMOS contacts of static random access memory (SRAM) array. Failure analysis (FA) results confirmed our prediction that they are P+/N-well junction leakages caused by nickel silicide (NiSi) spiking.

Introduction

Scanning electron microscope (SEM) [1] has been increasingly used in IC manufacturing in advanced technology node for defect inspection. WCMP is the most commonly used layer of EBI to detect contact open and gate or junction leakage.

Principle of charging modes of EBI at silicon device

The landing energy (LE) of EBI system usually is from few hundred eV to several keV. The relationship of LE and yield rate of the secondary electron (SE) and backscattered electron (BSE) are shown in Figure 1. [2] When $E_1 < LE < E_2$, more electrons leave surface than that reach it, which causes positive surface charging. When $LE > E_2$, less electrons leave surface than that reach it that causes negative surface charging. Because E_1 of the most materials are very low, most EBI systems don't operate at $LE < E_1$.

In WCMP EBI, e-beam two scans two materials: tungsten (W) and pre-metal dielectric (PMD). If e-beam LE less than E_2 of both materials, it is called positive mode EBI. Most WCMP EBI are using positive mode, which can effectively detect NMOS or gate leakage or short [3] and PMOS contact open [4]. Voltage contrast (VC) behaviors of W plugs that connect to different substrate at positive mode are illustrated in Figure 2a.

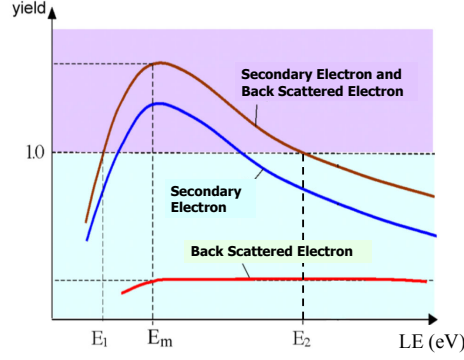


Figure 1. LE of e-beam and yield rate of SE and BSE.

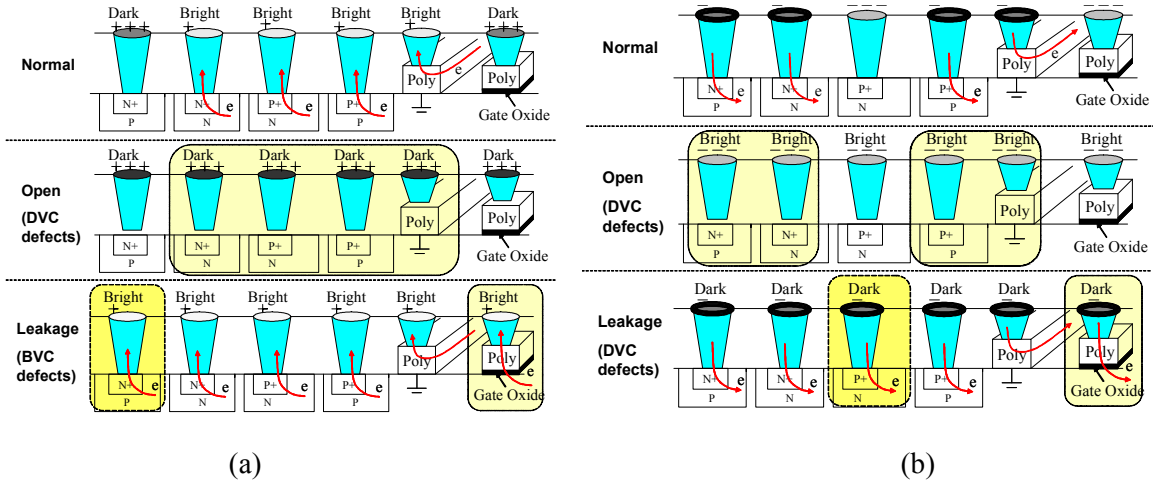


Figure 2. VC behaviors of W plugs at positive mode (a) and negative mode (b)

However, to detect other yield limiting defects, such as NMOS contact open, contact-to-poly short, and PMOS leakage/short, negative mode EBI is needed. Figure 2b illustrated VC behaviors of W plugs that connect to different substrate at negative mode.

Experiment and case study

In this experiment, we inspected two WCMP wafers on HMI's eScan[®]310, a high resolution (15 to 100 nm) EBI system. [5] The first wafer was prepared with slurry A. It was inspected at positive mode at first and we detected very high density of NMOS leakage, as show in Figure 3a as bright VC (BVC) defect. Then we tried to inspect it at negative mode. However, this wafer can't achieve it even at the maximum LE (3keV) of the EBI system, as show in Figure 6a. Even at 4.8 keV in an experimental system, it still showed mixed mode behavior, as shown in Figure 3b and 3c.

The mixed charging mode happened when PMD was negative charged while W was positively charged. In this case, a strong local electric field at the edge of PMD and grounded W plug is

formed. Few SE from that area can be collected by the detector because this local field, thus show a dark edge near the grounded W plug in SEM image.

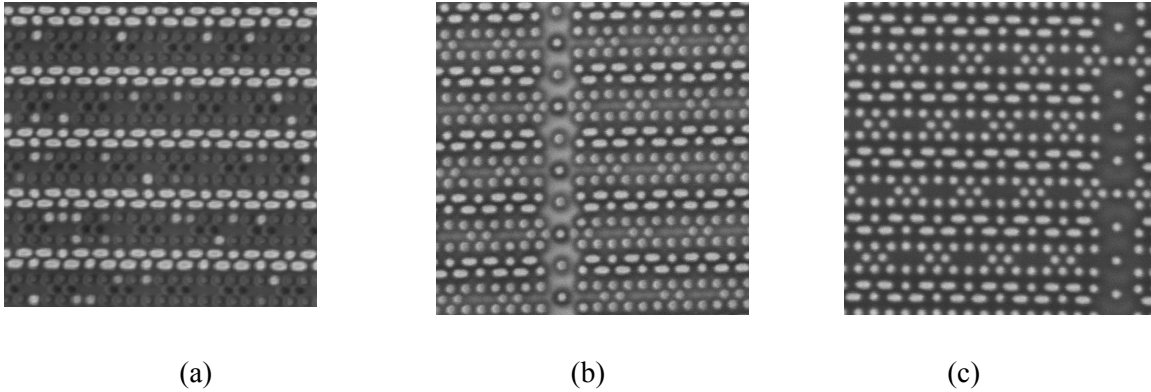


Figure 3. SRAM at positive mode 1.5 keV (a), mixed mode images at 3keV (b) and 4.8keV (c)

Surface condition related to WCMP process was strongly suspected for high E_2 of W in the first WCMP wafer. Cross-section Transmission electron microscope (TEM) image of Figure 4a shows about 200 to 250 Å W plug protrusion from PMD surface. This high W protrusion is likely the root-cause of high W E_2 . WCMP process using slurry B significantly reduced the W plug protrusion on the second WCMP wafer, as shown in Figure 4b and 4c. We also observed that the protrusion of W plug depends on the pattern density. At dense area, like N/PMOS CT, the W protrusion was almost reduced to zero, which resulted in E_2 value to less than 2 keV and created negative charging condition as we expected. On the contrary, in less dense area, like pass gate CT, it still had ~ 100 Å W protrusion, as shown in Figure 4c. We successfully achieved negative mode EBI on PMOS plugs of the second WCMP wafer, and detected PMOS DVC defects caused by P+/N-well leakage, as shown in Figure 5a. Figure 5b is the cross-section TEM image that reveals the cluster DVC is caused by NiSi spiking inducing source/drain to substrate short.

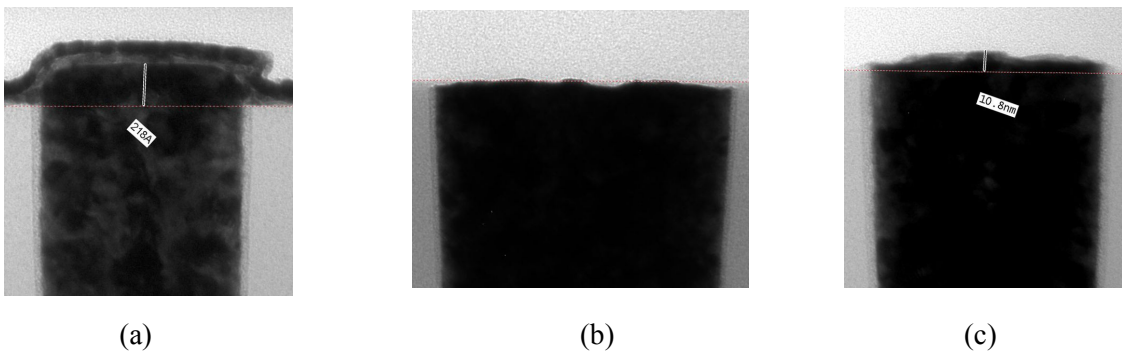


Figure 4. Slurry A: high W protrusion of pass gate plug (a). Slurry B: no W extrusion of oval plug (b) and medium W protrusion of pass gate plug (c).

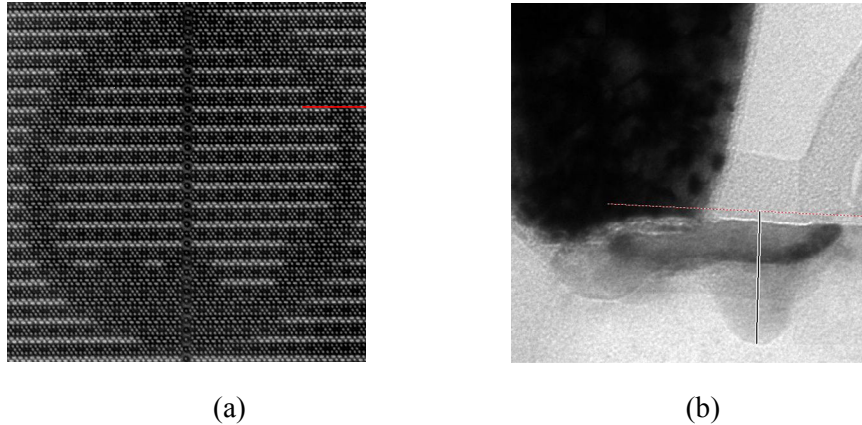


Figure 5. Negative mode DVC defects and FIB location (a) and cross-section TEM image (b)

Conclusions

We found that WCMP process can significantly affect EBI results because high W plug protrusion from PMD surface can cause high E_2 that affects W surface charging characteristics. Instead achieving negative mode, it reached mix mode at high LE, which can't be used to catch PMOS leakage. By changing WCMP slurry, we significantly reduced W protrusion and achieved negative mode EBI on WCMP wafer. Negative mode PMOS DVC defects were detected on SRAM. FA results confirmed that they are P+/N-well to substrate short caused by NiSi spiking.

Acknowledgement

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