E-beam Inspection for Gap Physical Defect Detection in 28nm CMOS Process

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***Abstract*—As design rule continuously shrinks, process windows narrow. Defects that are trivial in the previous technology node become yield limiting factors. E-beam inspection (EBI) starts to play a critical role in sub-design rule physical defect detection due to its superior resolution, high signal to noise ratio, and novel voltage contrast and material contrast capability. In this paper, we will demonstrate the application of EBI on three critical layers in 28nm CMOS process, covering from FEOL to BEOL.**

Keywords—EBI; CMOS; physical defect;

I. INTRODUCTION

As design rules shrink, defects that are trivial in previous generations become yield limiters for new technology nodes. According to the ITRS, defects as small as 20nm will become critical for 28nm CMOS processes. Inline detection of sub-design rule defects is critical for yield improvement in semiconductor manufacturing.

Traditionally, e-beam inspection (EBI) was widely used to detect electrical defects like opens or shorts in CMP layers. As the resolution of EBI tool improves, 5nm pixel size scanning is available in the state of the art EBI tool. As compared to Bright Field Inspection (BFI), EBI has several advantages, like superior resolution for sub-design rule defects (gap defects), sufficient quality of patch images for inline automated defect classification (ADC), and unique voltage contrast and material contrast. [1]

II. THIS PAPER WILL FOCUS ON THREE KEY EBI APPLICATIONS THAT COULD SIGNIFICANTLY LIMIT YIELD OF 28NM CMOS DEVICES USING THE HIGH-K METAL GATE (HKMG) PROCESS. CASE STUDIES

All studies conducted in this paper utilized the Hermes Microvision eScan320xp.

A. Abnormal SiGe Profile

The unique strained PMOS transistor structure, which features an epitaxial grown strained SiGe film embedded in the source drain regions, was first implemented in 90nm logic technology [2]. "A combination of compressive SiGe strain and embedded SiGe S/D geometry induces a large uniaxial compressive strain in the channel region, thereby resulting in significant hole mobility improvement."

In 28nm CMOS technology, profile abnormalities in selective epitaxial SiGe growth (SEG) may cause yield loss and reliability issues. The first experiment focused on the optimization of wet clean processes before the SiGe SEG process and concentration of Ge in the epitaxial process. Three wafers were used in the DOE. The process split conditions are listed in Table 1. A detailed process flow and EBI check point is illustrated in Figure 1. A 5nm pixel size was used in the EBI inspection and a dark defect was detected successfully and confirmed by TEM analysis. Figure 2 shows the defect review image and TEM image. Figure 3 shows the relationship between defective die percentage and process split conditions. From the EBI result, the split2 condition has much lower defective die percentage than split1 and baseline conditions. Yield results showed the same relationship as the EBI result. The high overfill induced SiGe growth from the spacer side wall and resulted in asymmetric growth. The improvement of the wet clean process and SiGe concentration increased yield by 15%.

TABLE I. PROCESS SPLIT CONDITIONS OF DOE ON WET CLEAN PROCESS AND SIGE EXPITAY PROCESS.

	BSL	Split 1	Split 2
SiGe concentration	Normal	+15%	+15%
Wet etch amount	Normal	Normal	+30%

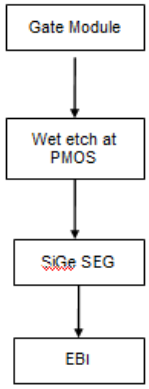

Fig. 1. Process flow of SiGe experiment and EBI check points

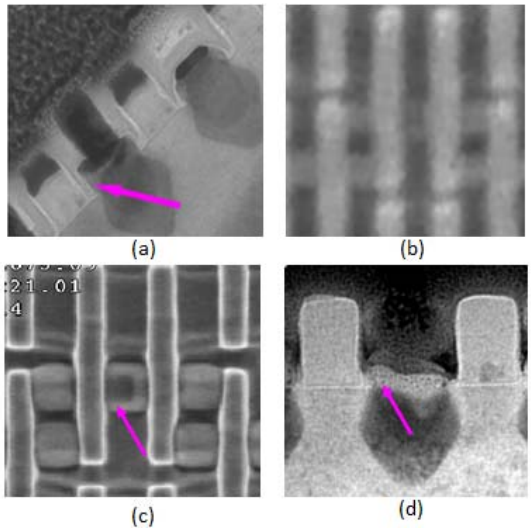

Fig. 2. Defect image and TEM analysis of SiGe abnormal. (a) FIB image; (b) Defect patch image from EBI; (c) Defect review image; (d) TEM image

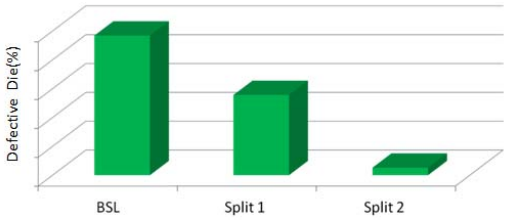

Fig. 3. Defective dies (%) for SiGe abnormal defect in 28 nm logic product.

B. NiSix Poor Formation

The quality of the salicide process determines the contact resistance and overall series resistance, which directly impacts device performance. Since the resolution of BFI is limited, it is advantageous to utilize EBI to detect poor NiSix formation.

Failure analysis results have shown that thinner NiSix at the bottom of via hole results in high resistance contacts or open circuits. Figure 4 shows a TEM result from failure analysis, an inline review image from the EBI tool, and its FIB analysis result.

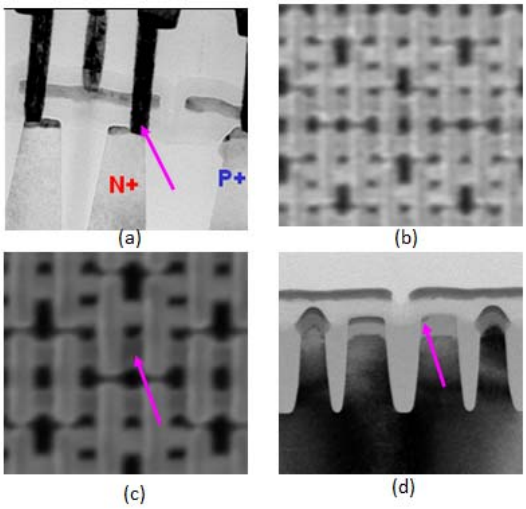

Fig. 4. Defect image and TEM analysis of NiSix poor formation. (a) TEM image; (b) Defect patch image from EBI; (c) Defect review image; (d) FIB image

Traditional failure analysis is performed after via WCMP (2 weeks after NiSix process), which leads to longer cycle time. In order to catch the defect earlier, EBI was utilized just after NiSi formation. A 5nm pixel size was used, and a dark defect was detected at the source and drain region. One hypothesis for the failure is a thicker SiN spacer creating a high aspect ratio structure that blocked the NiSix formation. Four wafers were used in the design of experiment (DOE) to check the dependency of defect performance against the thickness of SiN spacer. Table 2 shows the detailed DOE split conditions. One wafer used baseline process, and the other three wafers had different SiN thicknesses. Figure 5 illustrates the EBI results, which show a clear trend between the percentage of defective die and process split condition. The thinner the SiN spacer, the lower the percentage of defective dies have dark defects at the source and drain region. After optimization SiN (SW) process, yield can be improved 20% in the 28nm logic product.

TABLE II. PROCESS SPLIT CONDITIONS OF DOE ON THICKNESS OF SIN SPACER

	BSL	Split 1	Split 2	Split 3
SiN (SW) thickness	Normal	-15%	-30%	+15%

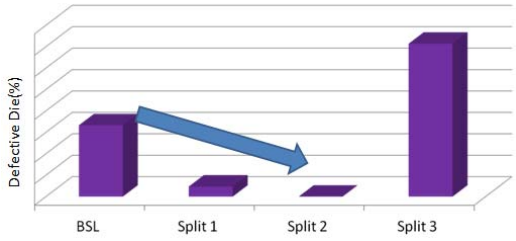

Fig. 5. Relationship between percentage of defective die and process split.

C. Cu Loss Problem After Dual-Damasence Process

Study [3] showed a decreased yield due to Cu loss problem based on a strong dependency on queue time between the etch process and wet clean process. A Cu oxidation model was created and illustrated that the fluorine catalyzed Cu oxidation at the via bottom after dual-damascene process will be removed by chemicals in the following wet clean process. Voids are formed at the bottom of the via that thereby decrease via connection yield.

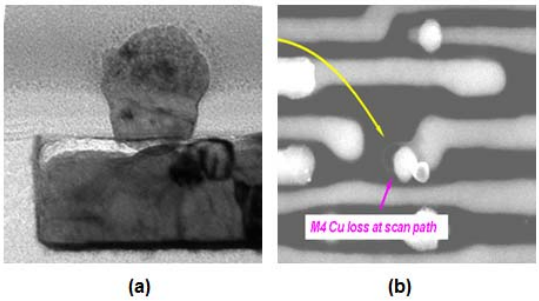

Fig. 6. Failure analysis result shows Cu loss in 28 nm logic product. (a). TEM Image; (b). SEM review image after delayered process

Since the Cu loss defect is small and is located at the bottom of via, it is difficult to detect with traditional inline defect inspection methodologies. CD-SEM or review SEM have been used to unveil Cu loss defect. Electrical test, which significantly lengthens the learning cycle, was used to quantify defective die percentage. In this work, a novel EBI methodology was utilized, which has been successfully implemented for Cu loss defect detection. Figure 7 shows defect patch image (a), review image (b), and defect map (c). TEM image (f) shows clear Cu loss on previous metal layer, which generates significant yield issue for 28nm process.

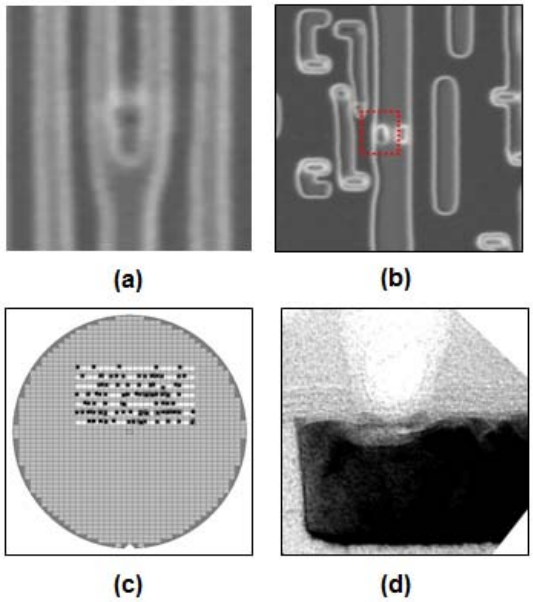

Fig. 7. EBI result for 28 nm logic product. (a). Defect patch image; (b). Defect review image; (c) Defect map; (d). TEM image shows Cu loss on previous metal layer.

This methodology is used to perform DOE study, and based on EBI results, we can figure out the best process condition from four splits. Moreover, a quantitative defective die percentage is also available for each split. Figure 8 illustrates the detailed process condition split for each wafer. As compared to the reference process, an extra scrubber process and DI rinse process can help reduce defective die percentage from around 70% to 15% and below 10%, respectively. 50% extension of post etch treatment time can help further decrease defective die percentage to 1% or less.

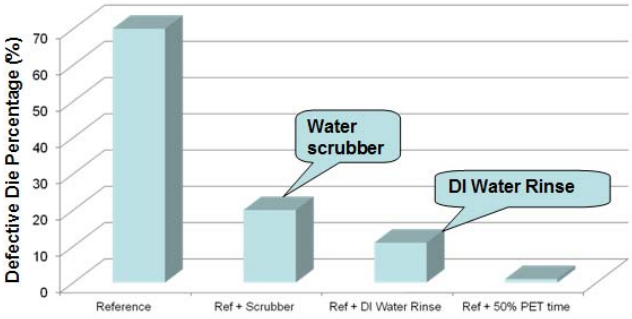

Fig. 8. Process conditions split and corresponding defective die percentage.

III. SUMMARY

As compared to BFI, EBI has several advantages, such as superior resolution for sub-design rule defects (gap defect), sufficient quality of patch images for inline ADC, and unique voltage contrast and material contrast. The successful implementation of EBI helps to significantly reduce learning cycles and starts to become an enabler for yield enhancement in the 28nm CMOS process.

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