Contact leakage and open monitoring with an advanced e-beam inspection system

Shuen-chen Lei[a], Hermes Liu[a], Mingsheng Tsai[a],
Hung-Chi Wu[b], Hong Xiao[c] and Jack Jau[c]

(a) Central Research Development, United Microelectronics Corp., No.18, Nanke 2nd Rd., Tainan Science Park, Tainan County 741, Taiwan, ROC
(b) Hermes Microvision, Inc., No. 18, Creation Road 1, Science Park, Hsinchu, Taiwan, ROC
(c) Hermes Microvision, Inc. USA, 1595 McCandless Drive, Milpitas, California, USA
Tel: 886-6-505-4888 Ext. 12138, Fax: 886-6-505-0960, E-mail: Shuen_Chen_Lei@umc.com

Abstract

In this study, we used optimized negative mode to detect N+/P-well contact open and P+/N-well contact leakage. We found the optimized contact process condition to eliminate both contact open and leakage. Electron beam (e-beam) inspection results strongly correlate with die yield. We implemented negative mode e-beam defect inspection along with positive mode inspection for effective inline monitoring to accelerate the 65 nm process yield ramp.

Introduction

E-beam defect inspection becomes more important at 65nm and 45nm technology nodes. Most e-beam inspections of tungsten chemical mechanical polish (WCMP) wafers are using positive mode (also called extraction mode) that can effectively detect P+/N-well open, gate leakage, and N+/P-well leakage. [1], [2] However, it is difficult to use positive mode to detect some other defects of interest (DOI), such as N+/P-well contact open and more importantly, P+/N-well leakage. The capability to detect these two DOI becomes especially important for 65 nm technology node yield ramp because there are different open root causes of N+/P-well from P+/N-well open and different leakage mechanism of P+/N-well from N+/P-well.

e-beam Inspection

Figure 1 is an illustration of e-Scan®300, an advanced e-beam inspection system used in this study. [3] The landing energy (LE) of e-beam can be controlled from 250 to 2500eV. The relationship of LE and yield rate of the secondary electron (SE), back scattered electron (BSE) and their combinations are shown in Figure 2. [4] When $E_1<LE<E_2$, more electrons leave surface than that reach surface, causing surface to charge positively. Inspection running in this regime is called positive mode inspection. When $LE>E_2$, less electrons leave surface than that reach surface, causing surface to charge negatively. Inspection running in this regime is called negative mode inspection, which is the focus of this study.

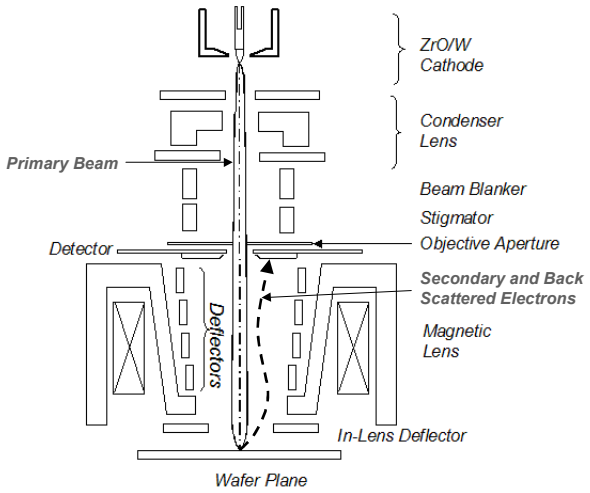


Figure 1. Schematics of the e-beam system of eScan®300.

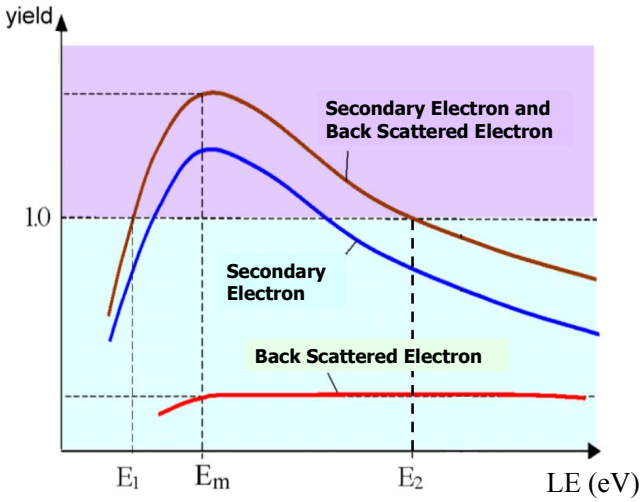


Figure 2. Relationship of LE of primary beam and SE and BSE yields.

At negative mode, PN junction of P+/N-well is reversely biased. Electrons are accumulated on the tungsten (W) plug surface, make it charge negatively and expel more SE to reach detector, therefore, its image in the SEM is bright. At the same time N+/P-well is forward biased, thus, most electrons leak to substrate, just as

it connects to the ground, causing the W plug that connects to it has lower gray level (GL) in SEM image. It also causes higher surface potential of this W plug than the surface potential of the surrounding negatively charged oxide. This potential difference introduces a strong local electric field between the ground W plugs and the oxide nearby. This strong local lateral field attracts SE from oxide to W plug and prevent them reach detector, resulting a dark ring near the ground or N+/P-well plug, as shown in Figure 3 and Figure 4a and 4b.

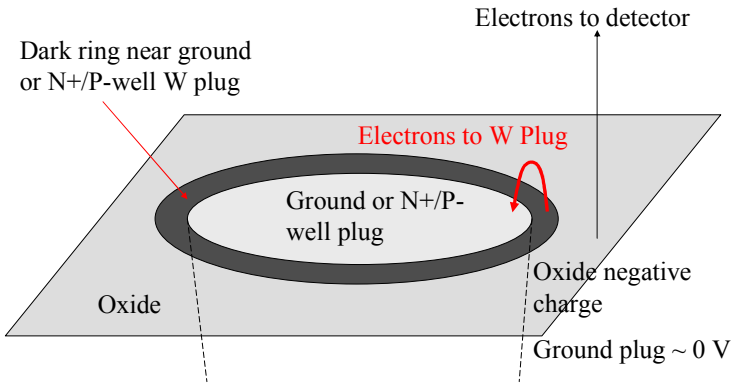
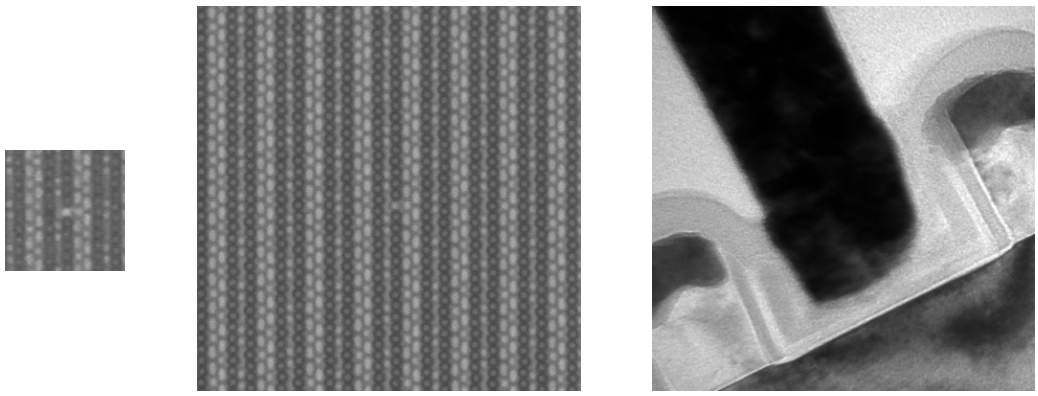


Figure 3. Explanation of dark ring near the ground plug at negative mode.

P+/N-well plug is normally bright without dark ring because the PN junction is reverse bias at negative mode and electrons can not leak to ground. When it has leakage, the plug will have lower GL while a dark ring will show up around it, allows us to detect dark voltage contrast (VC) defect. Similar, N+/P-well plug is normally dark with a dark ring. When the contact is open, the plug will become brighter and the dark ring will disappear, allow us to catch bright VC defect.

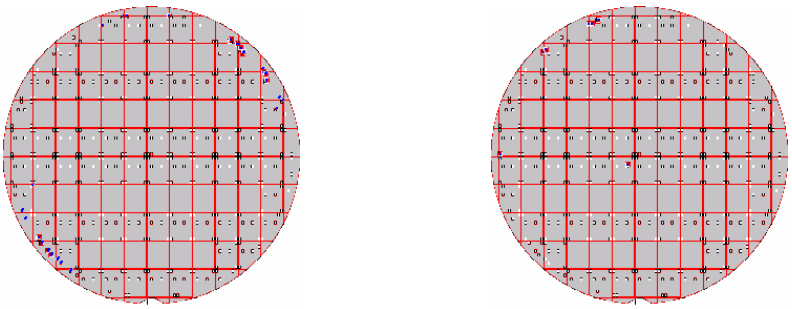
Results and Discussion

We used high landing energy to achieve negative mode on 65-nm wafer with W plugs. We've detected bright VC defects on N+/P-well plugs and cross-section TEM confirmed they are contact open. Figure 4a, 4b and 4c show the eScan®300 defect inspection patch image, eScan®300 defect review image, and the defect cross-section TEM image that shows a thin layer remain at the bottom of contact hole, respectively. This defect is difficult to detect at positive mode because N+/P-well plugs are normally dark and open defects show dark VC. [2] By optimizing etch process, we minimized this open defects, as shown in figure 5a and 5b.



(a) (b) (c)

Figure 4. (a) Defect inspection patch image, (b) review image the BVC defect, and (c) cross-sectional TEM image of the BVC defect.

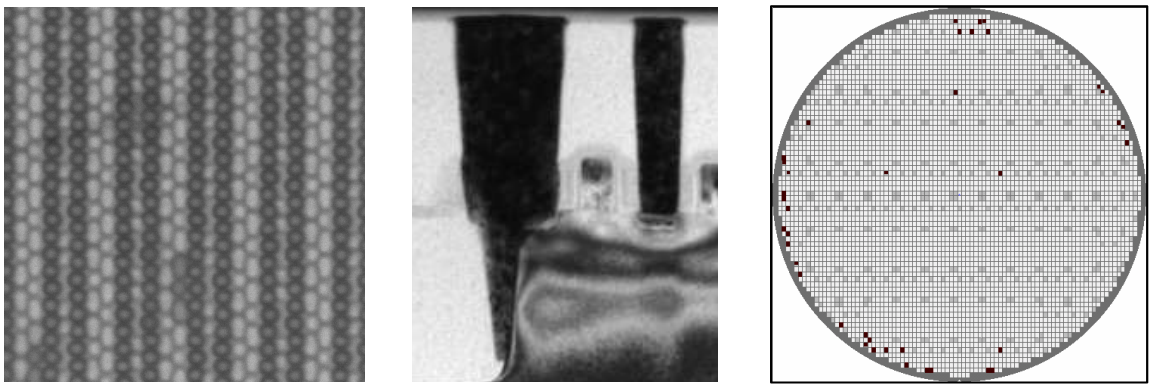


(a) (b)

Figure 5. N+/P-well contact BVC density: (a) with old recipe and (b) with new recipe.

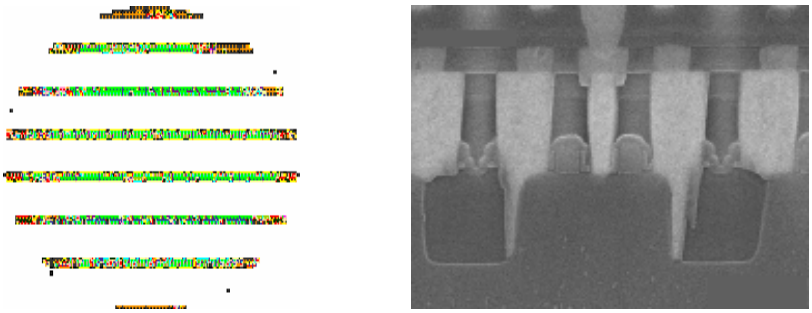
We've also detected dark VC defects on P+/N-well plugs and cross-section TEM shows they are leakage caused by W spiking due to layout and non-optimized etch. Figure 6a, 6b and 6c are review image of PMOS dark VC defect, cross-section TEM and DVC defect map that shown an edge high signature, respectively. This unique PMOS leakage defect is due to the layout and non-optimized etch process. It is very difficult to detect at positive mode because P+/N-well plugs normally are bright and leakage is bright VC. [1] Wafer acceptance test (WAT) also found leakage-induced yield loss, and the edge high leakage map correlated with the PMOS leakage (dark VC) defect map very well, as shown in Figure 7a. Failure analysis (FA) cross-

section SEM image showed the exactly same W spiking defects that caused the PMOS leakage, as shown Figure 7b.



(a) (b) (c)

Figure 6. (a) Review image of W-plugs with DVC defect, (b) cross-sectional TEM image of the defect (c) DVC defect map.



(a) (b)

Figure 7. (a) Final test leakage Map. (b) Cross-sectional SEM image of high leakage die.

By further optimize contact process, we successfully minimized this killer defect and improved product yield. We also implement this negative mode inspection for product line monitoring, as shown in Figure 8.

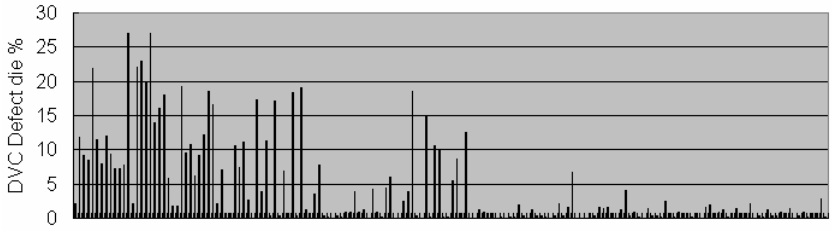


Figure 8. Inline monitoring of P+/N-well leakage DVC.

Conclusion

We have studied negative mode inspection of W filled contact wafers and detected N+/P-well open as bright VC defect and P+/N-well leakage as dark VC defect. Along with positive mode inspection that detects P+/N-well open (dark VC), N+/P-well leak (bright VC) and gate leak (bright VC), we've successfully implemented the in-line defect monitoring with an advance e-beam inspection system after WCMP to control most DOI and significantly improved 65 nm product yield.

Acknowledgement

Special thanks to Yung-chi Hsiao, Lucien Yeh and Yan Zhao of Hermes Microvision, Inc. for their strong supports.

References

(1) Hermes Liu, et al., Proceeding of the 31st International Symposium for Testing and Failure Analysis, pp. 448, 2005.
(2) Kirin Wang, et al., Proceeding of IEEE International Symposium of Semiconductor Manufacturing, pp. 472, 2005
(3) X. Liu, et al., J. Vac. Sci. Tech. B, **22**, pp.3534-3538, 2004.
(4) L. Reimer, "Scanning Electron Microscopy, Physics of Image Formation and Microanalysis", 2nd Ed., Springer, New York, 1998.